FIRE Emulator for H8S and H8/300H

Version 11-Nov-2014

```
F::d.l
 addr/line  code              label     mnemonic                  comment

       677           for ( i = 0 ; i <= SIZE ; i++ )
  P:010E6C  1955                       sub.w   r5,r5
  P:010E6E  79250012                   cmp.w   #12,r5             ; #18,r5
  P:010E72  4E3E                       bgt     10EB2
            {
       679                 if ( flags[ i ] )
  P:010E74  0D50                       mov.w   r5,r0
  P:010E76  17F0                       exts.l  er0
  P:010E78  78006A290020A3...          mov.b   @(20A37E,er0),r11; @(flags,er0)
```

```
F::r
Cy  C  ER0      16101  SP >00200000
V   _  ER1     20A390  +04 00010434
Zr  _  ER2     200000  +08 0001614E
Neg N  ER3          0  +0C 00010E4A
U   _  ER4          0  +10 00000000
H   H  ER5          0  +14 303A0020
UI  U  ER6     120000  +18 A0F20000
I   I  ER7     2104DC  +1C 00000009
IL  7  PC       10E72  +20 0001032A
Tsk    CCR        0E9  +24 00000000
       EXR         7F  +28 00000000
       MACH         0  +2C 00000000
       MACL         0  +30 00000000
```

```
F::v.w
flags = (1, 1, 1, 1, 1, 1, 1, 1, 1,
-`ast = (
  +'word = 0x0,
    count = 12346,
  +'left = 0x20A0F2,
  +'right = 0x0,
    field1 = 1,
    field2 = 2)
```

For general informations about the In-Circuit Debugger refer to the **"FIRE User´s Guide"** (fire_user.pdf). All general commands are described in **"IDE Reference Guide"** (ide_ref.pdf) and **"General Reference Guide"**.

NOTE:	Do not connect or remove probe from target while target power is ON. Power up: Switch on emulator first, then target Power down: Switch off target first, then emulator

Before debugging can be started, the emulator must be configured by software:

Ready to run setup files for most standard compilers can be found on the software CD in the directory **../Demo/H8S/Compiler**. All setup files are designed to run the emulator stand alone without target hardware.

The following description should make the initial setup (to run the emulator together with the target hardware) easier. It describes a typical setup with frequently used settings. It is recommended to use the programming language PRACTICE to create a batch file, which includes all necessary setup commands. PRACTICE files (*.cmm) can be created with the PRACTICE editor pedit (Command: **PEDIT <file name>**) or with any other text editor.

A basic setup file includes the following parts:

1. Set cpu-type and -mode
2. Set system options
3. Select dualport mode (optional)
4. Set mapper (optional)
5. Select frequency (optional)
6. Activate the emulator
7. Load application file (optional)
8. Set breakpoints (optional)
9. Start application
10. Stop application (optional)

Here a typical example, how to setup the system:

1. Set **cpu-type** and -**mode** options

   The command **sys.cpu** is used to select one derivative within a cpu-family and to set its operation mode.

```
system.down                  ; switch the system down
system.cpu H8S2655           ; select derivative H8S/2655
system.cpu EXP16M16          ; set the operation mode EXP16M16
```

2. Set **system options**

   The system window controls the CPU specific setup. Please check this window very carefully and set the appropriate options. Use the ↖? button in the main tool bar and click to the option check box (Command: **HELP.PICK**) to get online help in a pop up window.

```
system.option v33 on         ; on:  if a 3.3 V target board is used
system.option rame on        ; set RAME option corresponding to the
                             ; RAME bit in the SYSCR register
```

3. Select **dualport mode** (optional)

   Dualport allows access to emulation RAM, while emulation is running. This is necessary to display variables, set breakpoints or display the flag listings while the emulation is running. **System.Access** selects how dualport access is done.

```
system.access request        ; request: a dedicated bus request
                             ; signal of the bondout cpu is used
                             ; denied: dualport is disabled
```

4. Set **mapper** (optional)

   The mapper controls the memory access of the CPU. This means the use of internal or external memory, the protection of a memory bank etc. Address ranges must be defined by using **memory classes**.

```
map.reset                              ; reset mapper (all external)
map.ram c:0x0--0x07ffff                ; emulation RAM: 512KB (e.g. for
map.ram c:0x200000--0x23ffff           program)
map.intern c:0x0--0x07ffff             ; emulation RAM: 256KB (e.g. for
map.extern c:0x200000--0x23ffff        data)
                                       ; map program memory internal
                                       ; map data memory external
```

5. Select **frequency** (optional)

The CPU can be clocked by an internal (emulator) or external (target) clock source. If the internal clock is used, the clock is provides by the VCO of the emulator. The setting of the internal clock is done by the “vco” command.

The current CPU frequency can be displayed in the counter window (Command: **Count**).

```
vco.clock 20.                    ; input clock to the EXTAL pin of
                                 ; the cpu is set to 20 MHz (only
                                 ; necessary if internal clock is
                                 ; used)
```

6. Activate the emulator

When the emulator is activated a debug-monitor program is loaded into a hidden emulator memory. Afterwards, a bondout reset-signal is inactivated and the monitor program starts. This program allows access to user memory (data.dump, data.list) and cpu-registers, and gives control to start and stop the emulation.

```
system.mode emulext              ; system works with external target
                                 ; clock
```

7. **Load** application file (optional)

Application can be loaded by various file formats. UBROF format is often used to load code and symbol information. For information about the load command for your compiler see **Compiler.**

```
data.load.ubrof iarh8s.dbg       ; load application file
```

8. Set **breakpoints** (optional)

There are several ways to set breakpoints (Command: **Break.Set**). Breakpoints can be displayed using the **Break.List** command.

```
breakpoint.set main /program     ; set program break on function
                                 ; main
breakpoint.set flags /write      ; set write break on variable
                                 ; 'flags'
```

9. **Start** application

Application can be started with giving a break address. For example ***”go main”*** starts the application and stops at symbol main.

```
go                               ; run application
```

10. **Stop** application (optional)

    Application can be breaked manually by using th **BREAK** command.

```
break                                   ; break application manually
```

It is recommended to check the following chapters for all questions regarding the correct setup:

- **Configuration**
- **General SYStem Settings and Restrictions**
- **Special Settings and Restrictions of H8S/224x/23xx/265x**
- **Special Settings and Restrictions of H8S/21xx**
- **Special Settings and Restrictions of H8S/222x/223x/262x/263x**
- **Troubleshooting**

Hang-up

If you are not able to stop the emulation, there could be some typical reasons:

Active target-reset	The **BREAK** command won't stop the emulation if the target-reset is active and the reset-line is enabled in the exception control.
Hardware Standby Mode	The hardware standby mode can only be cancelled by a new activation (**sys.up**) of the emulator.

Dualport Errors

No information available.

Debugging via VPN	**The debugger is accessed via Internet/VPN and the performance is very slow. What can be done to improve debug performance?** The main cause for bad debug performance via Internet or VPN are low data throughput and high latency. The ways to improve performance by the debugger are limited: in practice scripts, use "SCREEN.OFF" at the beginning of the script and "SCREEN.ON" at the end. "SCREEN.OFF" will turn off screen updates. Please note that if your program stops (e.g. on error) without executing "SCREEN.OFF", some windows will not be updated. "SYStem.POLLING SLOW" will set a lower frequency for target state checks (e.g. power, reset, jtag state). It will take longer for the debugger to recognize that the core stopped on a breakpoint. "SETUP.URATE 1.s" will set the default update frequency of Data.List/ Data.dump/Variable windows to 1 second (the slowest possible setting). prevent unneeded memory accesses using "MAP.UPDATEONCE [address-range]" for RAM and "MAP.CONST [address--range]" for ROM/ FLASH. Address ranged with "MAP.UPDATEONCE" will read the specified address range only once after the core stopped at a breakpoint or manual break. "MAP.CONST" will read the specified address range only once per SYStem.Mode command (e.g. SYStem.Up).
H8S BurstROM Interface	**I can not map the BurstRom interface area to the emulation memory as internal.** The BurstROM interface can not be mapped as internal. The on-chip breakpoints must be used for the runtime control in an external BurstRom area.

Configuration

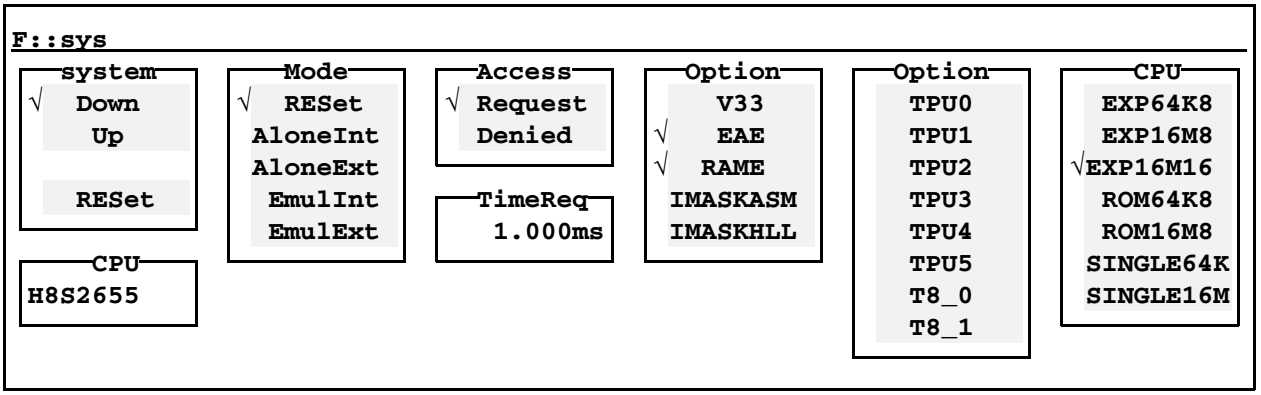
There is no special hardware configuration necessary for the H8S. The configuration of the used derivative and cpu-mode is done via the **SYSTEM** commands by software.

Emulation Method

The FIRE Emulator uses a bondout version of the H8S CPUs.

NOTE: The bondout chip replaces the target cpu, i.e. the target cpu must be removed during emulation!

Emulation Modes



The emulator can operate in 5 modes. The modes are selected by the **SYStem.Mode** command.

Format: **SYStem.Mode** <*mode*>

<*mode*>: **Reset**
AloneInt
AloneExt
EmulInt
EmulExt

Reset	CPU is in reset.
AloneInternal	CPU is running with internal clock. Bus strobe signals (AS, HWR, LWR, WAIT) are disabled. This mode is used for 'standalone' operation.
AloneExternal	CPU is running with external clock. Bus strobe signals are disabled.
Emulation Internal	CPU is running with internal clock. Bus strobe output signals are enabled.
Emulation External	CPU is running with external clock. Bus strobe output signals are enabled.

In active mode, the power of the target is sensed and by switching down the target the emulator changes to **RESET** mode. The probe is not supplied by the target power. When running without target, the target voltage is simulated by an internal pull-up resistor.

Dualport Access

Format:	**SYStem.MemAccess** <*option*>
<*option*>:	**Request** **Denied**

Request	The CPU bus access is stopped by a dedicated bondout bus-request signal for performing a dualport access.
Denied	Dualport access is not possible while the emulation is running.

Dualport allows access to emulation RAM and onchip ROM/FLASH/RAM of the cpu, while emulation is running. This is necessary to display variables, set breakpoints or display flag listings while the emulation is running. Dualport access is only possible on the emulators internal RAM and not on target RAM.

NOTE: The DTC-RAM is physically internal even at the bondout cpu. This means that this memory can't be changed via dualport access. All accesses of the cpu to the DTC-RAM are shadowed to an emulation RAM, so that the memory contents can be read via dualport.

Format: **SYStem.CpuAccess** <*option*>

<*option*>: **Enable**
Denied

Enable If a dualport read/write access is requested to a non-mapped memory, a spot point (emulation break and go) is used to access the memory.

Denied Dualport access via spot point is not possible.

The emulator uses a two stage strategy to realize “the best possible” dualport access method:

If MemAccess is set to Request, the emulation controller “tries” a bus arbitration access as dualport cycle. This is possible if memory is mapped to internal and on read cycles to shadow memory. Shadow memory means, that memory is mapped in the emulator (map.ram), but the area is mapped external (map.extern). On access to external mapped memory and write access to shadow memory the dualport is executed as a spot point if CpuAccess is enabled. Dualport on access to external mapped memory and write access to shadow memory is disabled if CpuAccess is disabled.

If MemAccess is set to Denied and CpuAccess is enabled, the emulation controller uses a spot point to realize the dualport cycle. If MemAccess is set to Denied and CpuAccess is disabled, dualport access is not possible.

The following table shows how the dualport is realized depending on the used system setting:

Mem Access	Cpu Access	Read Map Int.	Write Map Int.	Read Shadow	Write Shadow	Read Map Ext.	Write Map Ext.
Request	Enable	request	request	request	spot	spot	spot
Request	Denied	request	request	request	-	-	-
Denied	Enable	spot	spot	spot	spot	spot	spot
Denied	Denied	-	-	-	-	-	-

request: The bus arbitration interface of the CPU is used for dualport access. Application performance is only slightly influenced.

spot: The emulation is breaked, memory access is done via CPU, emulation is continued. Application performance decreases with this method.

General Restrictions

Onchip DTC-RAM	The CPUs onchip DTC-RAM is physically internal at the bondout chip. The write accesses of the CPU to the DTC area are shadowed to an emulator RAM, so that this shadow DTC-RAM can be read via dual-port, but there is no dualport write-access available to the DTC area. The CPU uses a 32-bit data transfer for reading and writing DTC register information, but only the lower 16 bit of the data can be seen in the trace (restriction of the bondout chip).
BurstROM interface	The BurstROM interface can't be mapped as internal. The **on-chip breakpoints** must be used for the runtime control in an external BurstRom area.
Interrupt requests during the emulation is stopped	Exceptions and interrupts are not handled during the emulation is stopped. Some of them are stored and executed after starting the emulation (see chapter **Exception Control**). If you will have problems with either your target hardware or you application program because of the blocked interrupts, then you have to use a foreground monitor.
Pending interrupts during single-step	When executing an assembler step and external or internal interrupts are pending, the emulator will step into the interrupt handler and stops at the first instruction of the interrupt service routine. The execution of the interrupt program can be avoided either by preventing the interrupt, e.g. stop the timer while the emulation is stopped (see **timer control**) or by masking the interrupt in the CPU (command **SETUP.IMASKASM**). For HLL steps the problem can be solved in the same way (command **SETUP.IMASKHLL**).

SYStem.Option V33 — 3.3 V power fail detection

Format: **SYStem.Option V33 [ON | OFF]**

The emulator has a detection logic to detect a target power fail. This option must be set to on, if a 3.3V target is used.

SYStem.Option RAME — Onchip RAM enable

Format:	**SYStem.Option RAME [ON | OFF]**

This option must be set corresponding to the *RAME* bit in the *SYSCR* register of the cpu. The emulator needs this information to set the breakpoints correctly.

SYStem.Option IMASKASM — Mask interrupts during assembler step

Format:	**SYStem.Option IMASKASM [ON | OFF]**

If enabled, the interrupt mask bits of the cpu will be set during assembler single-step operations. The interrupt routine is not executed during single-step operations. After single step the interrupt mask bits are restored to the value before the step.

SYStem.Option IMASKHLL — Mask interrupts during HLL step

Format:	**SYStem.Option IMASKHLL [ON | OFF]**

If enabled, the interrupt mask bits of the cpu will be set during HLL single-step operations. The interrupt routine is not executed during single-step operations. After single step the interrupt mask bits are restored to the value before the step.

NOTE:	By changing the status register through target software, this option can affect the flow of the target program. Accesses to the interrupt-mask bits will see the wrong values.

Continue with CPU specific Special Settings and Restrictions

The following Special Settings and Restrictions are different for the used bondout chip.

- **Special Settings and Restrictions of H8S/224x/23xx/265x**
- **Special Settings and Restrictions of H8S/21xx**
- **Special Settings and Restrictions of H8S/222x/223x/262x/263x**

Restrictions for H8S/224x/23xx/265x

Dual-purpose IO-Pins	The dual-purpose IO-Pins $\overline{\text{BREQ}}$, IRQ0..7 and $\overline{\text{WAIT}}$ don't have a pull-up resistor in the emulator. This pins work as port pins after reset. If you change the pin functions so that this pins have bus control or interrupt function, then the emulator will malfunction in stand-alone mode because of the floating inputs.

SYStem.CPU — Processor type

Format: **SYStem.CPU** <type>

<type>: **H8S2240 | H8S2241 | H8S2242 | H8S2243 | H8S2244 | H8S2245 | H8S2246**
H8S2340 | H8S2341 | H8S2343 | H8S2345
H8S2350 | H8S2351 | H8S2352 | H8S2353 | H8S2355 | H8S2357
H8S2653 | H8S2655
H8S2310| H8S2311 | H8S2312 | H8S2316| H8S2318
H8S2320| H8S2322 | H8S2323 | H8S2324| H8S2327 | H8S2328| H8S2329
H8S2332 | H8S2337 | H8S2338| H8S2339

This selects the exact derivative within a CPU family.

Format: **SYStem.CPU** <mode>

<mode>: **EXP64K8**
EXP16M8
EXP16M16
ROM64K8
ROM16M8
SINGLE64K
SINGLE16M

This option specifies operation mode of the cpu, which is normally defined with the MD0..2 pins of the cpu. But, the values of this pins in the target are **not** responsible for the operation mode, so that the pin levels can differ from the emulator setting.

EXP64K8 Expanded mode with 64 KByte address range, 8-bit initial bus width and onchip ROM disabled

EXP16M8 Expanded mode with 16 MByte address range, 8-bit initial bus width and onchip ROM disabled

EXP16M16 Expanded mode with 16 MByte address range, 16-bit initial bus width and onchip ROM disabled

ROM64K8 Expanded mode with 64 KByte address range, 8-bit initial bus width and onchip ROM enabled

ROM16M8 Expanded mode with 16 MByte address range, 8-bit initial bus width and onchip ROM enabled

SINGLE64K Single-chip mode with 64 KByte address range

SINGLE16M Single-chip mode with 16 MByte address range

SYStem.Option EAE External address enable

Format: **SYStem.Option EAE [ON | OFF]**

This option must be set corresponding to the *EAE* bit in the *BCRL* register of the cpu. The emulator needs this information to set the breakpoints correctly.

Format: **SYStem.Option TPU<channel> [ON | OFF]**

<channel>: **0 | 1 | 2 | 3 | 4 | 5**

This option controls the timers of the CPUs Timer Pulse Unit for each channel independently.

Normally, the timers continue running if the emulation is stopped. If the option is now switched **on**, the corresponding timer will stop after entering the break mode and will start running again before the emulation is started. This is done by manipulating the timer start register by the emulators background monitor program. Since there have to be done some important actions in the monitor before the timer control, the starting and stopping can't be synchronous to the emulators "go" and "break".

SYStem.Option T8 Control of 8-bit timer unit

Format: **SYStem.Option T8_<channel> [ON | OFF]**

<channel>: **0 | 1**

This option controls the timers of the CPUs 8-bit timers for each channel independently (see **SYStem.Option TPU**)

Restrictions for H8S/21xx

Dual-purpose IO-Pins	The dual-purpose IO-Pins $\overline{\text{BREQ}}$ and $\overline{\text{IRQ0..7}}$ and don't have a pull-up resistor in the emulator. This pins work as port pins after reset. If you change the pin functions so that this pins have bus control or interrupt function, then the emulator will malfunction in stand-alone mode because of the floating inputs.

SYStem.CPU Processor type

Format: **SYStem.CPU** <type>

<type>: **H8S2120 | H8S2122 | H8S2123 | H8S2124 | H8S2126 | H8S2127 | H8S2128**
H8S2130 | H8S2132 | H8S2133 | H8S2134 | H8S2137 | H8S2138
H8S2142 | H8S2143 | H8S2144 | H8S2147 | H8S2148

This selects the exact derivative within a CPU family.

SYStem.CPU Operation mode

Format: **SYStem.CPU** <mode>

<mode>: **EXP64K8**
SINGLE64K
SINGLE16M

This option specifies operation mode of the cpu, which is normally defined with the MD0..1 pins of the cpu. But, the values of this pins in the target are **not** responsible for the operation mode, so that the pin levels can differ from the emulator setting.

EXP64K8 Expanded mode with 64 KByte address range, 8-bit initial bus width and onchip ROM disabled

SINGLE64K Single-chip mode with 64 KByte address range

SINGLE16M Single-chip mode with 16 MByte address range

The *EXPE* bit in the *MDCR* register must be set to 1 in order to use external addresses.

Restrictions for H8S/222x/223x/262x/263x

Dual-purpose IO-Pins	The dual-purpose IO-Pins $\overline{\text{BREQ}}$, IRQ0..7 and $\overline{\text{WAIT}}$ don't have a pull-up resistor in the emulator. This pins work as port pins after reset. If you change the pin functions so that this pins have bus control or interrupt function, then the emulator will malfunction in stand-alone mode because of the floating inputs.

SYStem.CPU — Processor type

Format:	**SYStem.CPU** <type>
<type>:	**H8S2223 | H8S2225 | H8S2227 | H8S2233 | H8S2235 | H8S2236 | H8S2237 | H8S2238** **H8S2621 | H8S2622 | H8S2623| H8S2626 | H8S2631 | H8S2632 H8S2633** **H8S2636**

This selects the exact derivative within a CPU family.

Format: **SYStem.CPU** <mode>

<mode>: **EXP16M8**
EXP16M16
ROM16M8
SINGLE16M

This option specifies operation mode of the cpu, which is normally defined with the MD0..2 pins of the cpu. But, the values of this pins in the target are **not** responsible for the operation mode, so that the pin levels can differ from the emulator setting.

EXP16M8 Expanded mode with 16 MByte address range, 8-bit initial bus width and onchip ROM disabled

EXP16M16 Expanded mode with 16 MByte address range, 16-bit initial bus width and onchip ROM disabled

ROM16M8 Expanded mode with 16 MByte address range, 8-bit initial bus width and onchip ROM enabled

SINGLE16M Single-chip mode with 16 MByte address range

SYStem.Option SUBCLK Subclock enable

Format: **SYStem.Option SUBCLK [ON | OFF]**

If this option is on, then a 32,768 kHz subclock is fed into the pin *OSC1*, otherwise it is tied to VCC. The *OSC1* pin from the target is ignored. To avoid monitor timeout, waitstates should not be used in subclock mode.

SYStem.Option TPU Control of timer pulse unit

Format: **SYStem.Option TPU<channel> [ON | OFF]**

<channel>: **0 | 1 | 2 | 3 | 4 | 5**

This option controls the timers of the CPUs Timer Pulse Unit for each channel independently.

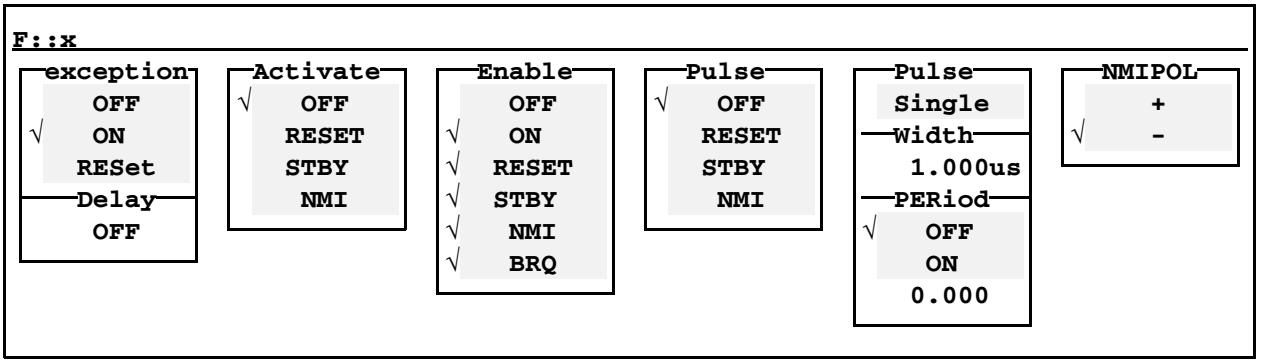
Normally, the timers continue running if the emulation is stopped. If the option is now switched **on**, the corresponding timer will stop after entering the break mode and will start running again before the emulation is started. This is done by manipulating the timer start register by the emulators background monitor program. Since there have to be done some important actions in the monitor before the timer control, the starting and stopping can't be synchronous to the emulators "go" and "break".

SYStem.Option T8 — Control of 8-bit timer unit

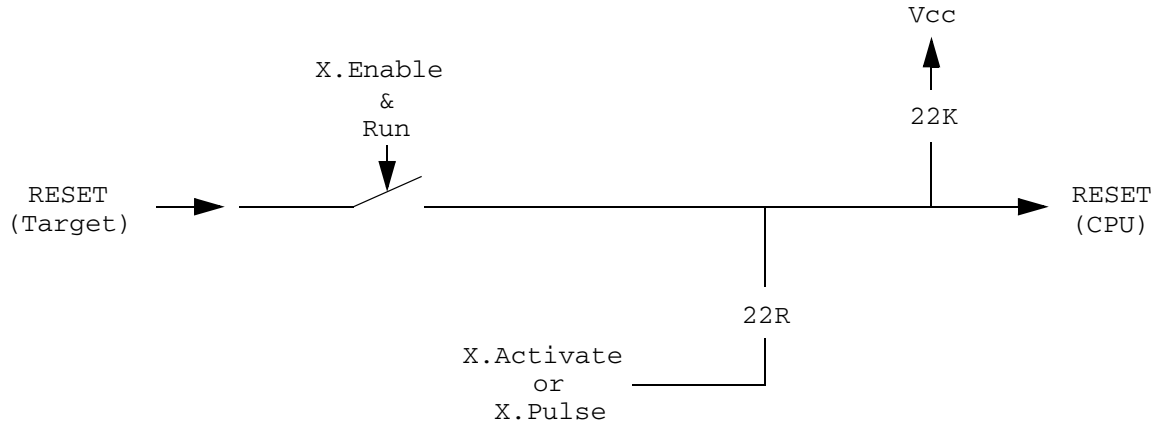
Format:	**SYStem.Option T8_<channel> [ON | OFF]**
<channel>:	**0 | 1 | 2 | 3**

This option controls the timers of the CPUs 8-bit timers for each channel independently (see **SYStem.Option TPU**)

Exception Control



Reset



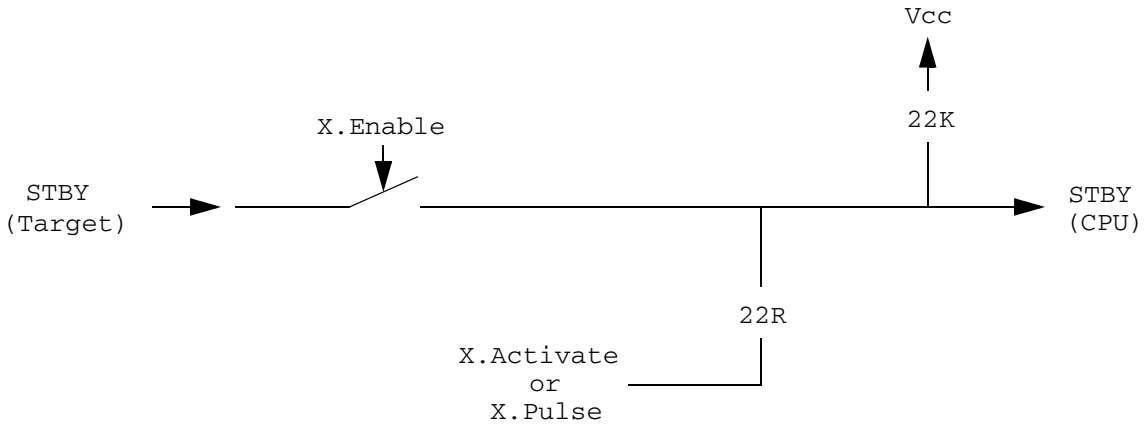
Format:	**eXception.Enable RESET [ON | OFF]**

Enable or disable external RESET line.

Format:	**eXception.Activate RESET[ON | OFF]**

Set RESET line active or inactive.

NOTE: The reset-line is driven low by the emulator, if the emulator is in system-down mode!

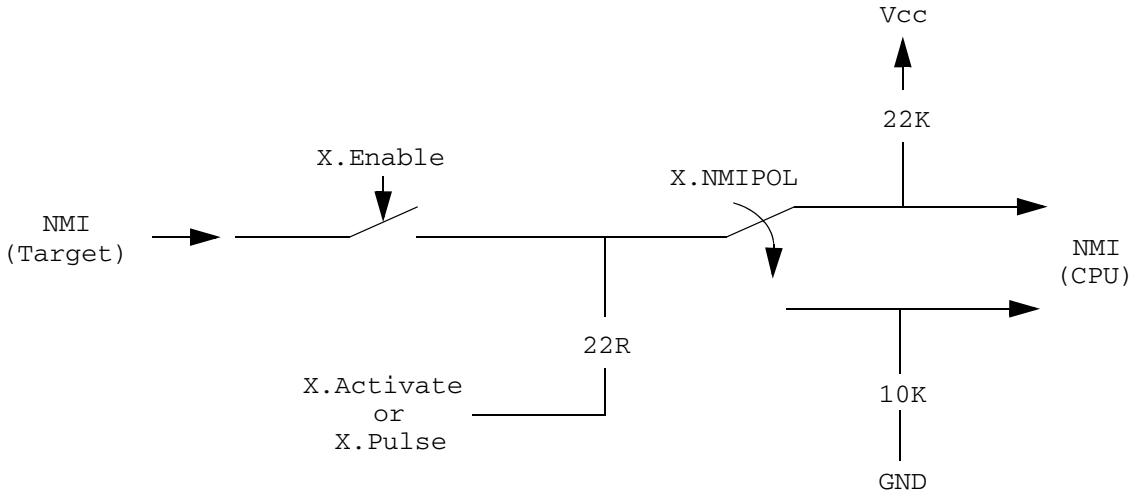


Format:	**eXception.Enable STBY [ON | OFF]**

Enable or disable external STBY line.

Format:	**eXception.Activate STBY [ON | OFF]**

Set STBY line active or inactive.



Format:	**eXception.Enable NMI [ON | OFF]**

Enable or disable external NMI line.

Format:	**eXception.Activate NMI [ON | OFF]**

Set NMI line active or inactive.

Format:	**eXception.NMIPOL [+ | -]**

Selects the NMI edge. Set it corresponding to the bit *NMIE* in the System Control Register *SYSCR* of the CPU.

-
Selects the falling edge and the 22K pull-up resistor is active (see drawing above).

+
Selects the rising edge and the 10K pull-down resistor is active (see drawing above).

Exceptions during Break Mode

During break mode (application program not running), the hardware-caused exceptions are controlled by the bondout CPU.

NMI

If a NMI occurs, then it is stored in the CPU. So, exception processing will occur after the first instruction of the started emulation.

External level sensitive interrupts

If a level sensitive interrupt occurs, then it is not stored in the CPU. So, interrupt processing will not occur if the /IRQ pin is not asserted until the emulation is started.

External edge sensitive interrupts

If an edge sensitive interrupt occurs, then it is stored in the CPU. So, interrupt processing will occur after the first instruction of the started emulation.

Internal interrupts

If an internal interrupt occurs, then it is stored in the CPU. So, interrupt processing will occur after the first instruction of the started emulation.

Breakpoints

For a basic description of the **breakpoint system** please refer to FIRE User's Guide.

Breakpoint Realization Modes

This chapter describes the different realization modes and shows their availability for the logical breakpoints types.

Software Breakpoints

Synchronous Breakpoints:
The user application code is patched with a special break-instruction of the bondout CPU (opcode 0x5770) before jumping into the user program. After executing this instruction, the CPU stops the user program and jumps into the emulator debug monitor.
NOTE: A synchronous software breakpoint in the onchip DTC-RAM area can't be set while the application is running.
Asynchronous Breakpoints:
These breakpoints are used as address selectors for the trigger unit (see **FIRE User's Guide**).

Hardware Breakpoints

Synchronous Breakpoints:
The user application is stopped before the instruction is executed. For this, the bondout break opcode is switched to the CPU data-bus instead of the user application opcode via hardware. This type of breakpoint is useful if you would like to set a breakpoint in a target memory where no code can be patched (e.g. EPROM or Flash).
NOTE: This breakpoint type doesn't work in the onchip ROM and RAM area. There are only synchronous software breakpoints available.
Asynchronous Breakpoints: See **FIRE User's Guide**).

Onchip Breakpoints

The bondout CPU has an onchip trigger-unit with two independent channels.
Synchronous Breakpoints:
They can be used if you would like to set a breakpoint in a target memory where no code can be patched (e.g. EPROM, Flash or BurstROM).
NOTE: The breakpoint is a "break after make", and not a "break before make".
Asynchronous Breakpoints:
They work only on data read or write cycles, not on instruction fetches. The information, that a breakpoint has occurred is switched from the bondout break controller to the emulator trigger unit, so that the trigger unit for example can start the analyzer (with special **keywords**).
There is a fixed connection between the breakpoint types and the channels:
'Alpha' corresponds to channel A
'Beta' corresponds to channel B

The following table shows realization of the logical breakpoint types in auto-mode.

Breakpoint Type	Realization in Auto Mode
Program	Software
HLL	Software Onchip (If the address is mapped as ReadOnly) Stepmode (If HLL-Line is too complex)
Spot	Software Onchip (If the address is mapped as ReadOnly)
Read, Write	Onchip
Alpha, Beta, Charly, Delta, Echo	Hardware

Overview

Access Class	Description
C	CPU (Program and Data)
D	Data
P	Program
ED	Dualport Data
EP	Dualport Program

C:, E:, D:, P:, ED:, EP:

C:, P: and D:

This storage classes operate on the same physical memory. They are only used to be compatible with other emulation probes.

E:, EP: and ED:

The E: prefix is used for accesses via dualport. The onchip I/O-registers and the onchip DTC-RAM area can’t be accessed via dualport.

Restrictions

Word access to external 8-bit bus	It is shown in the trace list as one bus cycle. The timestamp is shows the two bus cycles.

Keywords for the Display

AREA	Access area
STATE	CPU status
ASELIR	Instruction fetch
ASELID1	Instruction decode 1
ASELID2	Instruction decode 2
ASEBCCB	Branch not taken
ASEPFC	Prefetch cancel

Keywords for the Emulator Trigger Unit

General H8S Keywords for the Emulator Trigger Unit

Input Event	Meaning	Analyzer hardware FEC
BTA	Condition match of onchip trigger-unit channel A	X
BTB	Condition match of onchip trigger-unit channel B	X
DATA	Data access	X
FETCH	Prefetch cycle	X
Read	Read access	X
Write	Write access	X

H8S/224x/23xx/265x Keywords for the Emulator Trigger Unit

Input Event	Meaning	Analyzer	hardware
		FEC	
none			

H8S/21xx Keywords for the Emulator Trigger Unit

Input Event	Meaning	Analyzer	hardware
		FEC	
none			

H8S/222x/223x/262x/263x Keywords for the Emulator Trigger Unit

Input event	Meaning	Analyzer	hardware
		FEC	
none			

For not CPU-specific keywords, see **non-declarable input variables** in **"Analyzer Trigger Unit Programming Guide"** (analyzer_prog.pdf).

Port Signals H8_30XX

Name	Group	Description
P10 .. P17	P1	Port P10 .. P17
P20 .. P27	P2	Port P20 .. P27
P30 .. P37	P3	Port P30 .. P37
P40 .. P47	P4	Port P40 .. P47
P50 .. P57	P5	Port P50 .. P57
P60 .. P67	P6	Port P60 .. P67
P70 .. P77	P7	Port P70 .. P77
P80 .. P84	P8	Port P80 .. P84
P90 .. P95	P9	Port P90 .. P95
PA0 .. PA7	PA	Port PA0 .. PA7
PB0 .. PB7	PB	Port PB0 .. PB7
PC0 .. PC7	PC	Port PC0 .. PC7

Port Signals H8S_212X

Name	Group	Description
P10 .. P17	P1	Port P10 .. P17
P20 .. P27	P2	Port P20 .. P27
P30 .. P37	P3	Port P30 .. P37
P40 .. P47	P4	Port P40 .. P47
P50 .. P52	P5	Port P50 .. P52
P60 .. P67	P6	Port P60 .. P67
P70 .. P77	P7	Port P70 .. P77

Port Signals H8S_213X

Name	Group	Description
P10 .. P17	P1	Port P10 .. P17
P20 .. P27	P2	Port P20 .. P27
P30 .. P37	P3	Port P30 .. P37
P40 .. P47	P4	Port P40 .. P47
P50 .. P52	P5	Port P50 .. P52
P60 .. P67	P6	Port P60 .. P67

Name	Group	Description
P70 .. P77	P7	Port P70 .. P77
P80 .. P86	P8	Port P80 .. P86
P90 .. P97	P9	Port P90 .. P97

Port Signals H8S_214X

Name	Group	Description
P10 .. P17	P1	Port P10 .. P17
P20 .. P27	P2	Port P20 .. P27
P30 .. P37	P3	Port P30 .. P37
P40 .. P47	P4	Port P40 .. P47
P50 .. P52	P5	Port P50 .. P52
P60 .. P67	P6	Port P60 .. P67
P70 .. P77	P7	Port P70 .. P77
P80 .. P86	P8	Port P80 .. P86
P90 .. P97	P9	Port P90 .. P97
PA0 .. PA7	PA	Port PA0 .. PA7
PB0 .. PB7	PB	Port PB0 .. PB7

Port Signals H8S_222X/H8S_223X

Name	Group	Description
P10 .. P17	P1	Port P10 .. P17
P30 .. P36	P3	Port P30 .. P36
P40 .. P47	P4	Port P40 .. P47
P70 .. P77	P7	Port P70 .. P77
P96 .. P97	P9	Port P96 .. P97
PA0 .. PA3	PA	Port PA0 .. PA3
PB0 .. PB7	PB	Port PB0 .. PB7
PC0 .. PC7	PC	Port PC0 .. PC7
PD0 .. PD7	PD	Port PD0 .. PD7
PE0 .. PE7	PE	Port PE0 .. PE7
PF0 .. PF7	PF	Port PF0 .. PF7
PG0 .. PG4	PG	Port PG0 .. PG4

Port Signals H8S_224X

Name	Group	Description
P10 .. P17	P1	Port P10 .. P17
P20 .. P27	P2	Port P20 .. P27
P30 .. P35	P3	Port P30 .. P35
P40 .. P43	P4	Port P40 .. P43
P50 .. P53	P5	Port P50 .. P53
PA0 .. PA3	PA	Port PA0 .. PA3
PB0 .. PB7	PB	Port PB0 .. PB7
PC0 .. PC7	PC	Port PC0 .. PC7
PD0 .. PD7	PD	Port PD0 .. PD7
PE0 .. PE7	PE	Port PE0 .. PE7
PF0 .. PF7	PF	Port PF0 .. PF7
PG0 .. PG4	PG	Port PG0 .. PG4

Port Signals H8S_232X

Name	Group	Description
P10 .. P17	P1	Port P10 .. P17
P20 .. P27	P2	Port P20 .. P27
P30 .. P35	P3	Port P30 .. P35
P40 .. P47	P4	Port P40 .. P47
P50 .. P57	P5	Port P50 .. P57
P60 .. P67	P6	Port P60 .. P67
PA0 .. PA7	PA	Port PA0 .. PA7
PB0 .. PB7	PB	Port PB0 .. PB7
PC0 .. PC7	PC	Port PC0 .. PC7
PD0 .. PD7	PD	Port PD0 .. PD7
PE0 .. PE7	PE	Port PE0 .. PE7
PF0 .. PF7	PF	Port PF0 .. PF7
PG0 .. PG4	PG	Port PG0 .. PG4

Port Signals H8S_233X

Name	Group	Description
P10 .. P17	P1	Port P10 .. P17
P20 .. P27	P2	Port P20 .. P27
P30 .. P35	P3	Port P30 .. P35
P40 .. P47	P4	Port P40 .. P47
P50 .. P57	P5	Port P50 .. P57
P60 .. P67	P6	Port P60 .. P67

Name	Group	Description
P70 .. P75	P7	Port P70 .. P75
P80 .. P86	P8	Port P80 .. P86
P92 .. P97	P9	Port P92 .. P97
PA0 .. PA7	PA	Port PA0 .. PA7
PB0 .. PB7	PB	Port PB0 .. PB7
PC0 .. PC7	PC	Port PC0 .. PC7
PD0 .. PD7	PD	Port PD0 .. PD7
PE0 .. PE7	PE	Port PE0 .. PE7
PF0 .. PF7	PF	Port PF0 .. PF7
PG0 .. PG4	PG	Port PG0 .. PG4

Port Signals H8S_235X/H8S_265X

Name	Group	Description
P10 .. P17	P1	Port P10 .. P17
P20 .. P27	P2	Port P20 .. P27
P30 .. P35	P3	Port P30 .. P35
P40 .. P47	P4	Port P40 .. P47
P50 .. P53	P5	Port P50 .. P53
P60 .. P67	P6	Port P60 .. P67
PA0 .. PA7	PA	Port PA0 .. PA7
PB0 .. PB7	PB	Port PB0 .. PB7
PC0 .. PC7	PC	Port PC0 .. PC7
PD0 .. PD7	PD	Port PD0 .. PD7
PE0 .. PE7	PE	Port PE0 .. PE7
PF0 .. PF7	PF	Port PF0 .. PF7
PG0 .. PG4	PG	Port PG0 .. PG4

Port Signals H8S_262X

Name	Group	Description
P10 .. P17	P1	Port P10 .. P17
P40 .. P47	P4	Port P40 .. P47
P90 .. P97	P9	Port P90 .. P97
PA0 .. PA5	PA	Port PA0 .. PA5
PB0 .. PB7	PB	Port PB0 .. PB7
PC0 .. PC7	PC	Port PC0 .. PC7
PD0 .. PD7	PD	Port PD0 .. PD7
PE0 .. PE7	PE	Port PE0 .. PE7
PF0 .. PF7	PF	Port PF0 .. PF7

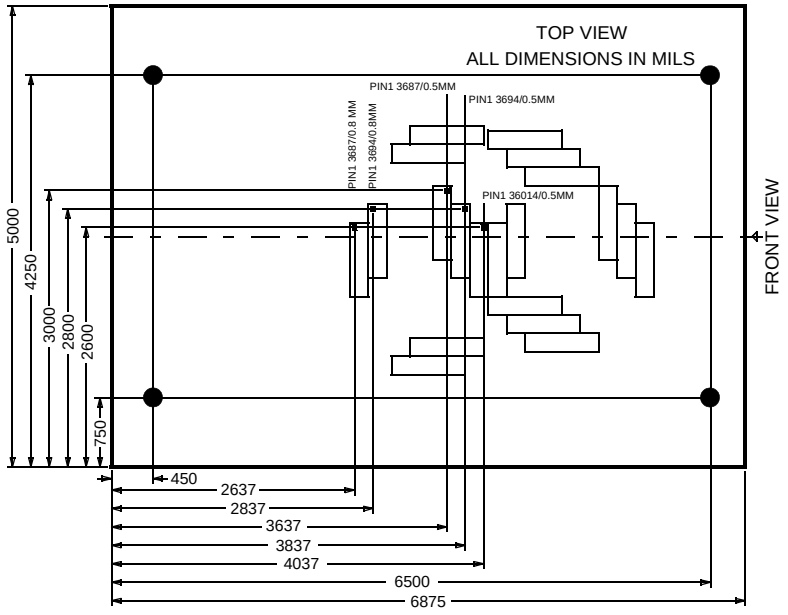
Port Signals H8S_2636

Name	Group	Description
P10 .. P17	P1	Port P10 .. P17
P30 .. P35	P3	Port P30 .. P35
P40 .. P47	P4	Port P40 .. P47
P90 .. P93	P9	Port P90 .. P93
PA0 .. PA3	PA	Port PA0 .. PA3
PB0 .. PB7	PB	Port PB0 .. PB7
PC0 .. PC7	PC	Port PC0 .. PC7
PD0 .. PD7	PD	Port PD0 .. PD7
PE0 .. PE7	PE	Port PE0 .. PE7
PF0	PF	Port PF0
PF3 .. PF7	PF	Port PF3 .. PF7

Port Signals H8S_263X

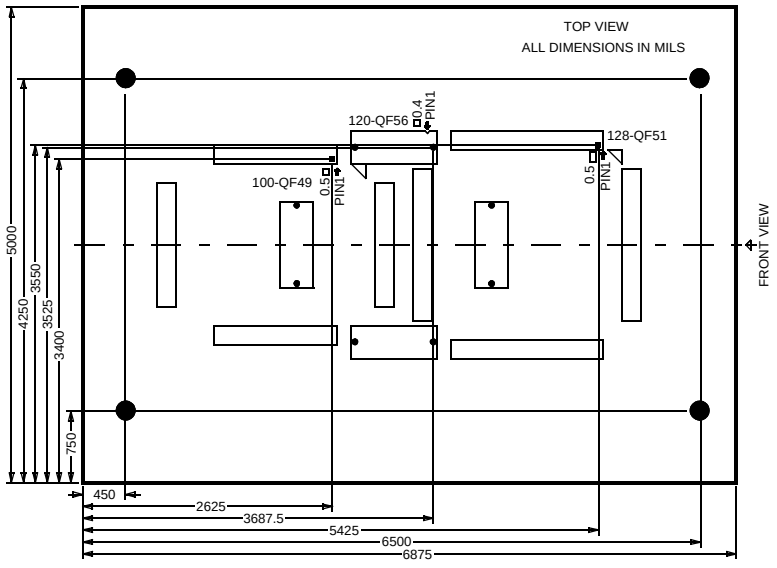
Name	Group	Description
P10 .. P17	P1	Port P10 .. P17
P30 .. P37	P3	Port P30 .. P37
P40 .. P47	P4	Port P40 .. P47
P70 .. P77	P7	Port P70 .. P77
P90 .. P97	P9	Port P90 .. P97
PA0 .. PA7	PA	Port PA0 .. PA7
PB0 .. PB7	PB	Port PB0 .. PB7
PC0 .. PC7	PC	Port PC0 .. PC7
PD0 .. PD7	PD	Port PD0 .. PD7
PE0 .. PE7	PE	Port PE0 .. PE7
PF0 .. PF7	PF	Port PF0 .. PF7
PG0 .. PG4	PG	Port PG0 .. PG4

Mechanical Dimensions

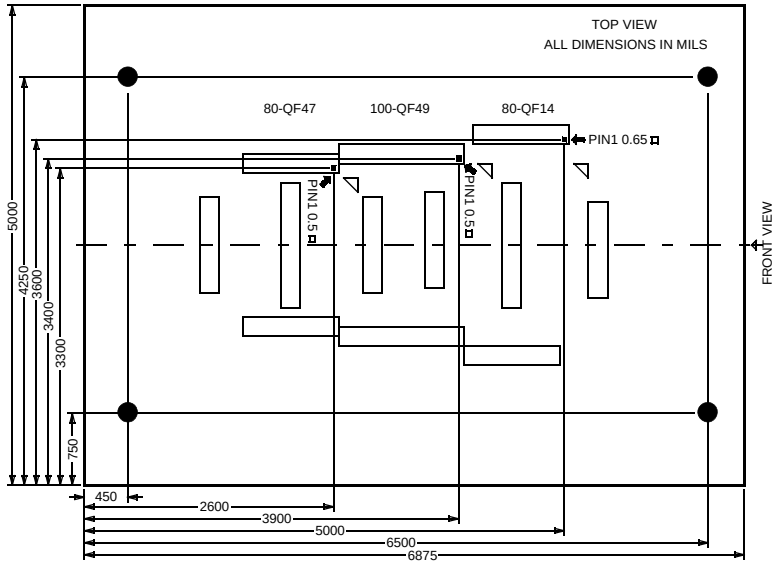
Dimension
LA-9569 FIRE-M-H8S-11

LA-9570 FIRE-H8S

Dimension

LA-9571 FIRE-M-H8S-1

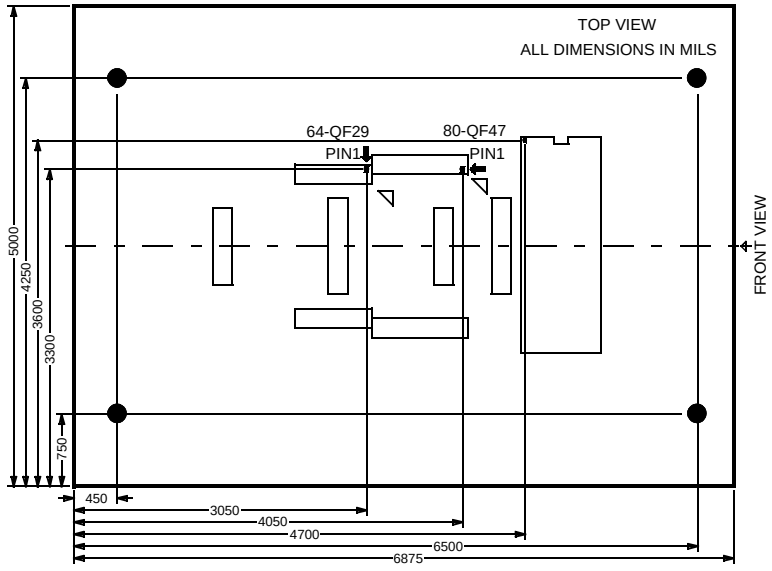


LA-9572 FIRE-M-H8S-2

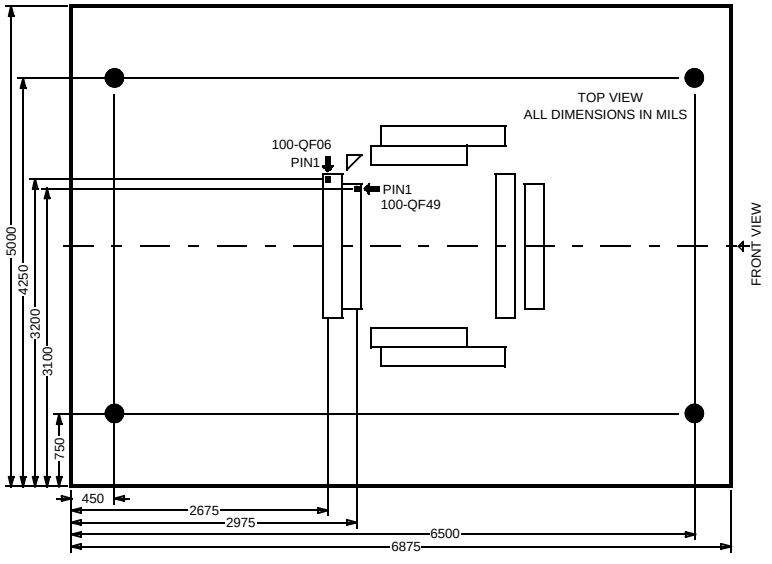


Dimension

LA-9573 FIRE-M-H8S-3

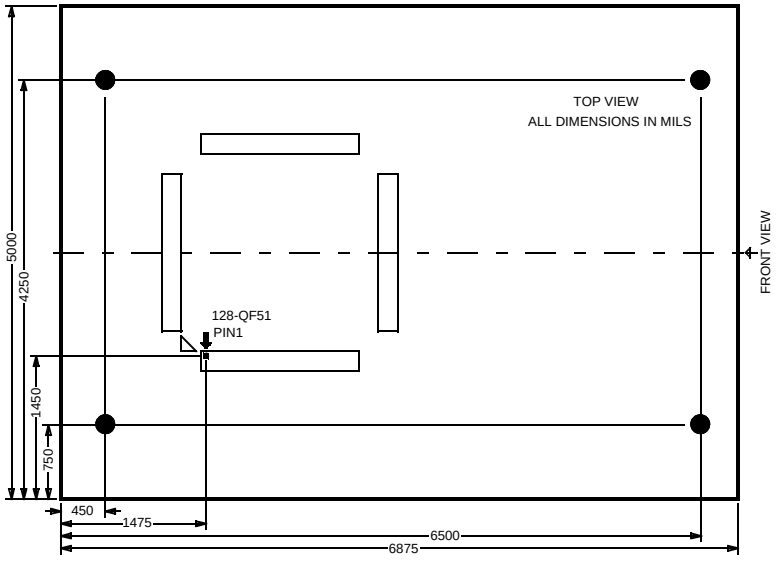


LA-9574 FIRE-M-H8S-4

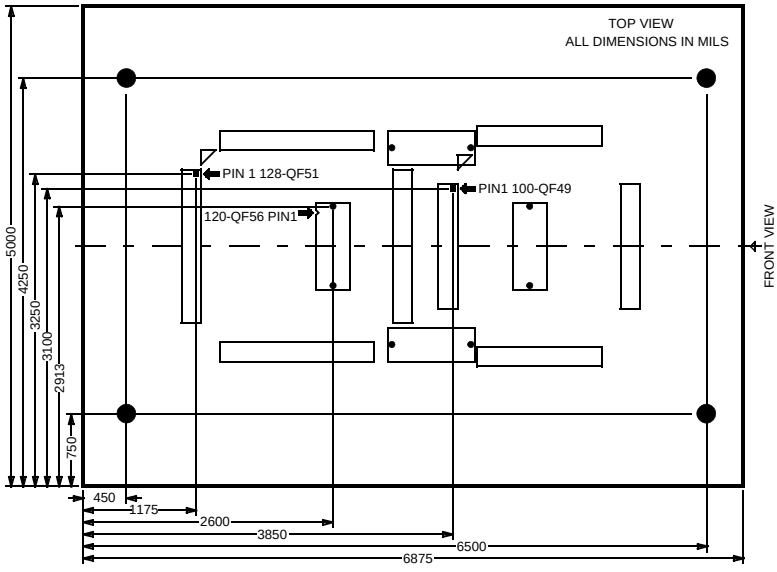


Dimension

LA-9575 FIRE-M-H8S-5

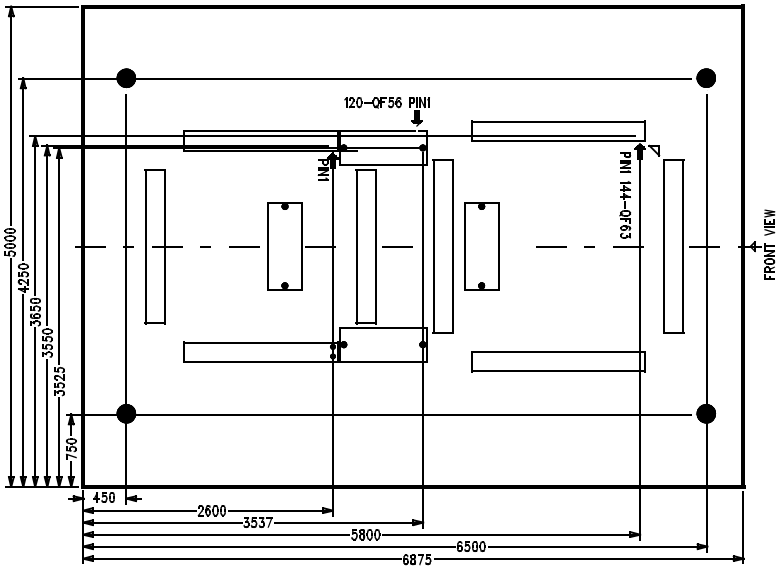


LA-9576 FIRE-M-H8S-6

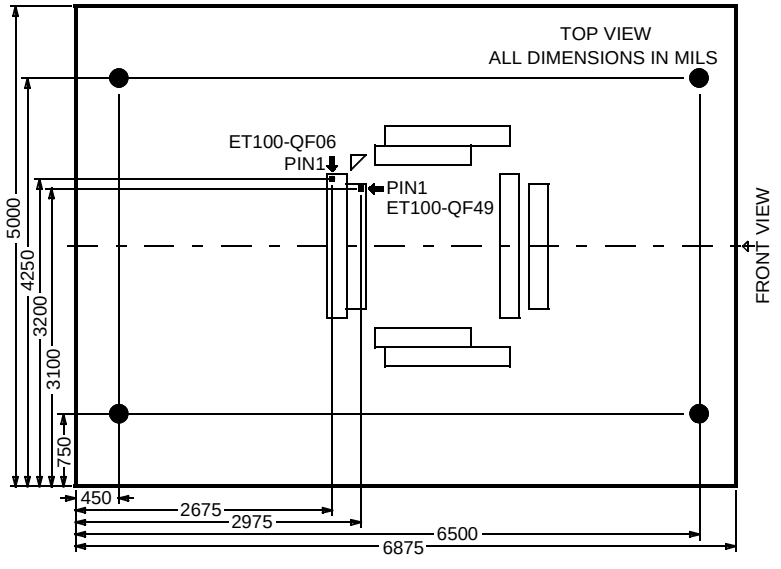


Dimension

LA-9577 FIRE-M-H8S-7

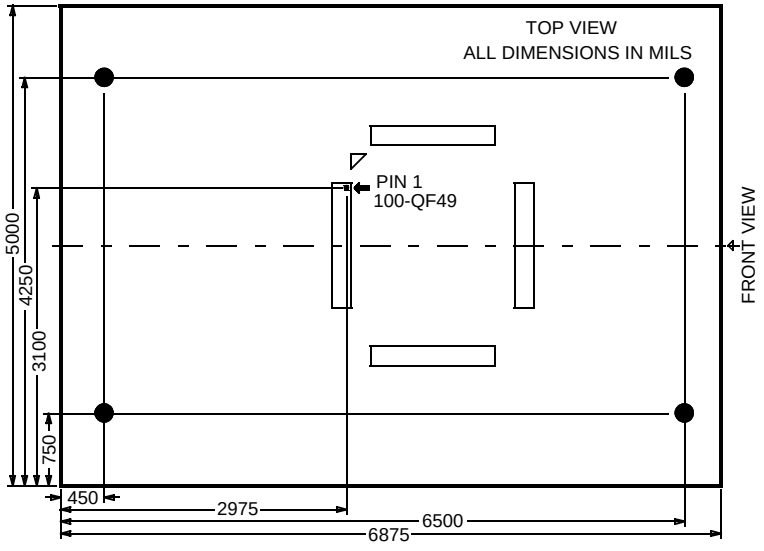


LA-9578 FIRE-M-H8S-8

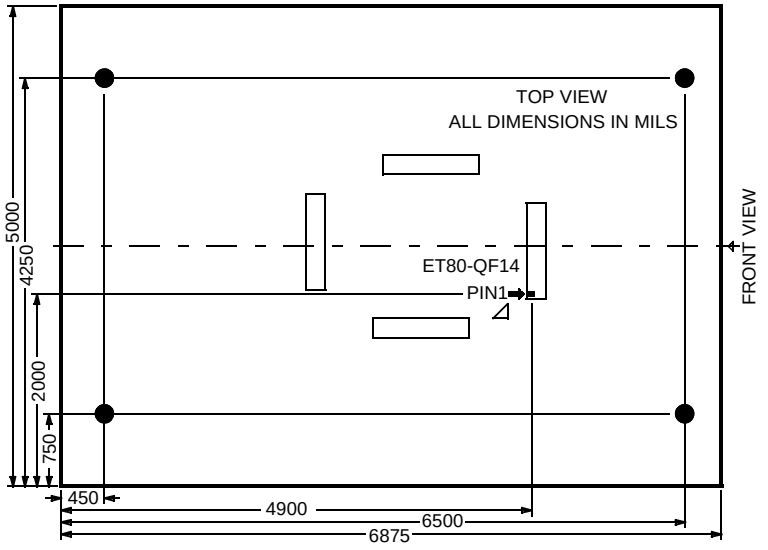


Dimension

LA-9579 FIRE-M-H8S-9

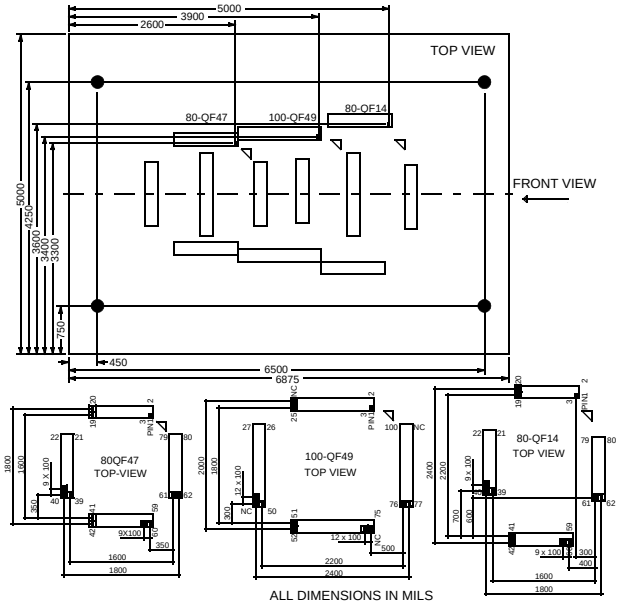


LA-9580 FIRE-M-H8S-10

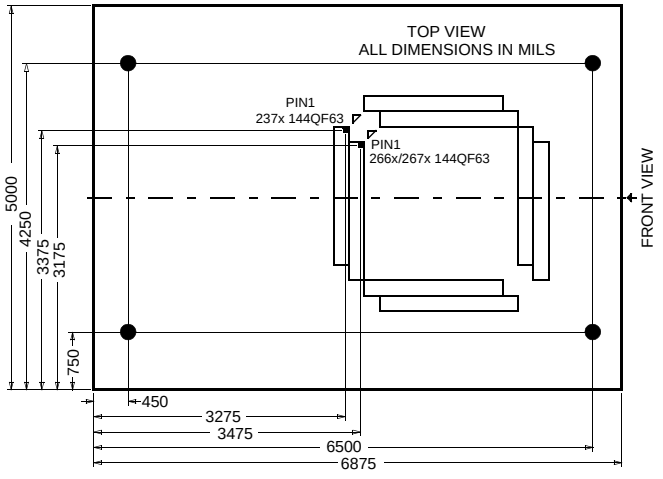


Dimension

LA-9586 FIRE-M-H8S-12

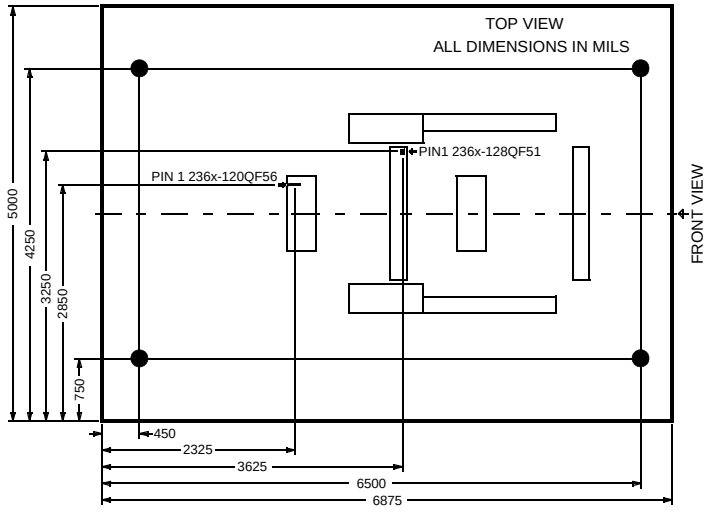


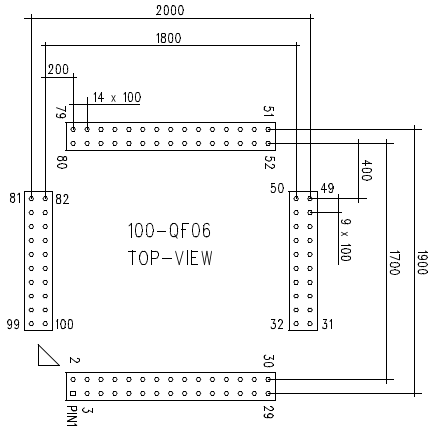
LA-9587 FIRE-M-H8S-13

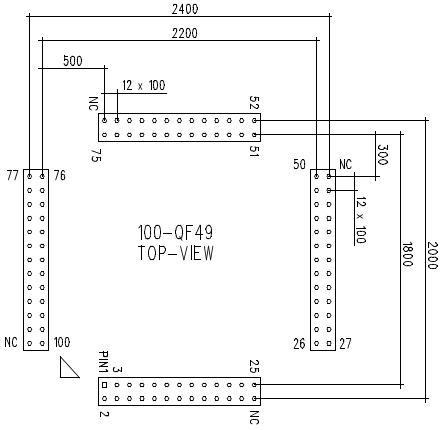


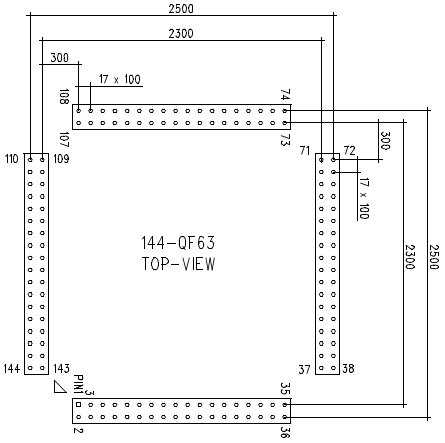
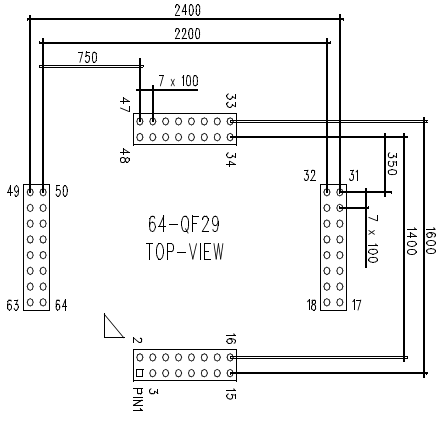
Dimension

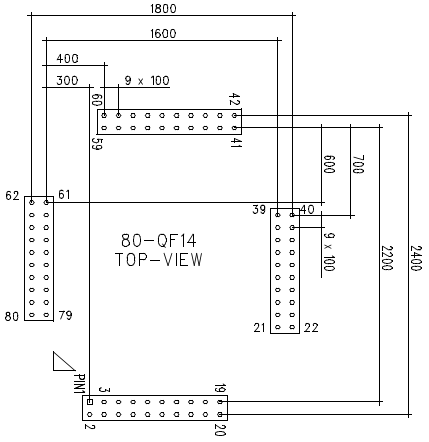
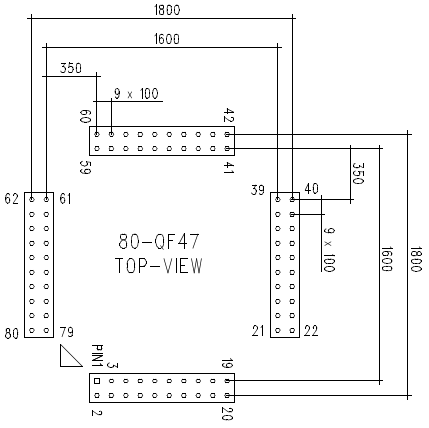
LA-9588 FIRE-M-H8S-14

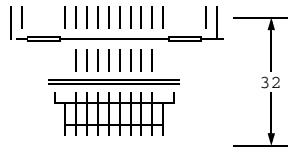
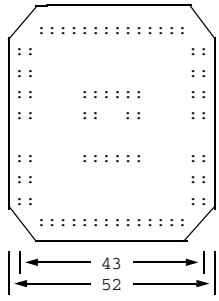


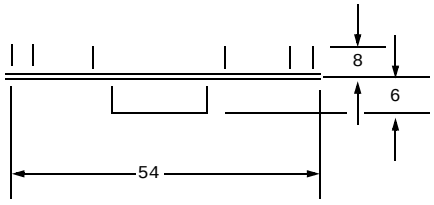
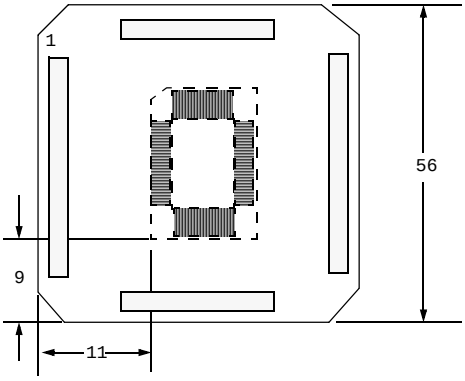
CPU	Adaption
H8S/2214 H8S/2223 H8S/2223 H8S/2225 H8S/2225 H8S/2227 H8S/2227 H8S/2233 H8S/2233 H8S/2235 H8S/2235 H8S/2236 H8S/2236 H8S/2237 H8S/2237 H8S/2238 H8S/2238	**ET100-QF06** 

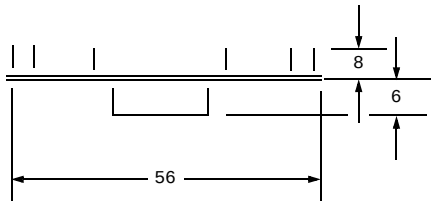
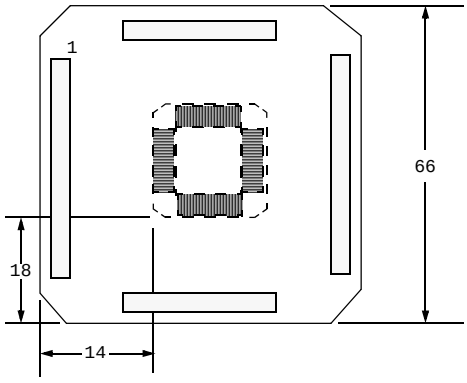
CPU	Adaption
H8/3006 H8/3007 H8/3008 H8/3044 H8/3045 H8/3046 H8/3047 H8/3048 H8/3052 H8/3060 H8/3061 H8/3062 H8/3064 H8/3065 H8/3066 H8/3067 H8/3068 H8S/2142 H8S/2143 H8S/2144 H8S/2147 H8S/2148 H8S/2214 H8S/2223 H8S/2223 H8S/2225 H8S/2225 H8S/2227 H8S/2227 H8S/2233 H8S/2233 H8S/2235 H8S/2235 H8S/2236 H8S/2236 H8S/2237 H8S/2237 H8S/2238 H8S/2238 H8S/2240 H8S/2241 H8S/2242 H8S/2243 H8S/2244 H8S/2245 H8S/2246 H8S/2310 H8S/2311 H8S/2312 H8S/2316 H8S/2318 H8S/2319 H8S/2340 H8S/2341 H8S/2343 H8S/2345	**ET100-QF49** 

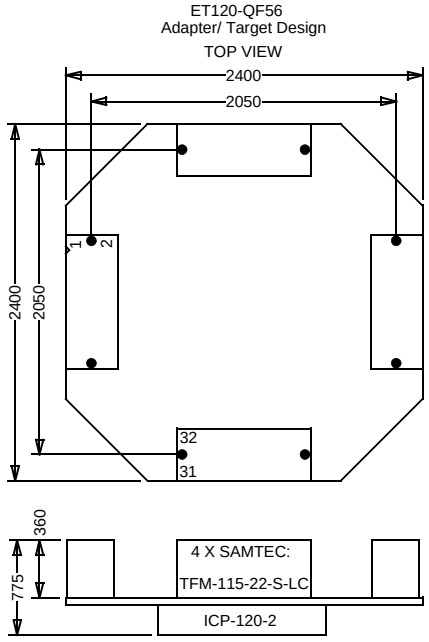
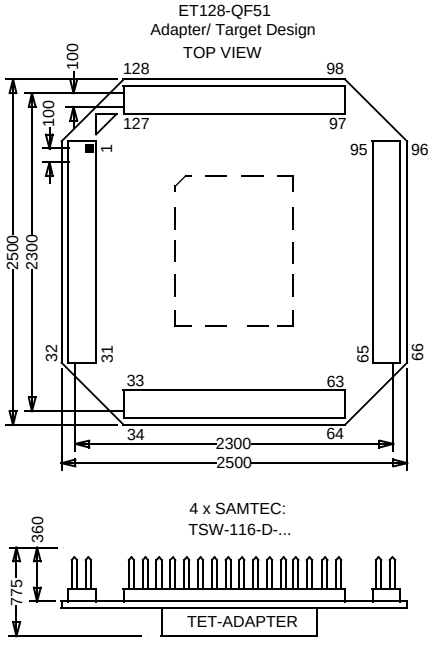
CPU	Adaption
H8S/2332 H8S/2337 H8S/2338 H8S/2339	**ET144-QF63** 
H8/36014 H8/3664 H8/3672 H8/3687 H8/3694 H8S/2120 H8S/2122 H8S/2123 H8S/2124 H8S/2126 H8S/2127 H8S/2128	**ET64-QF29** 

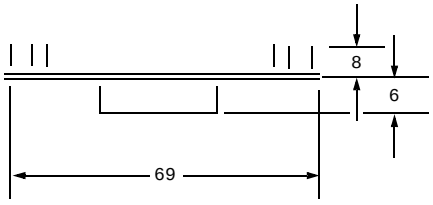
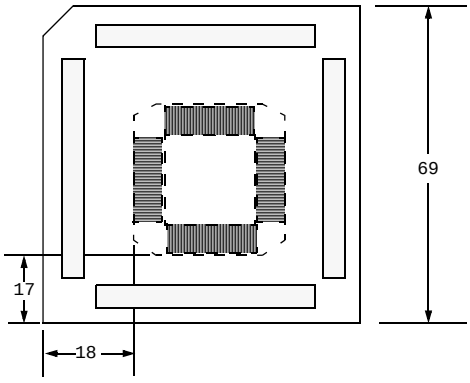
CPU	Adaption
H8S/2130 H8S/2132 H8S/2133 H8S/2134 H8S/2137 H8S/2138 H8S/2612	**ET80-QF14** 
H8S/2120 H8S/2122 H8S/2123 H8S/2124 H8S/2126 H8S/2127 H8S/2128 H8S/2130 H8S/2132 H8S/2133 H8S/2134 H8S/2137 H8S/2138	**ET80-QF47** 

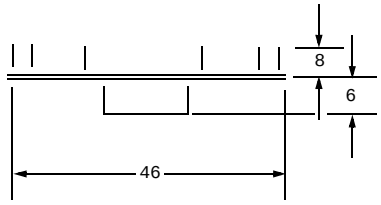
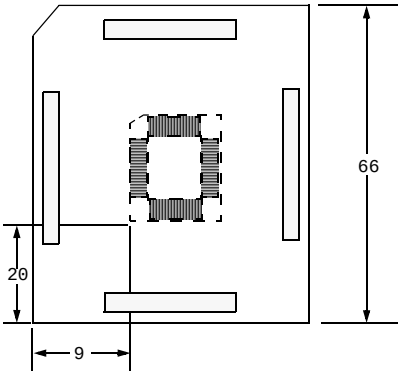
Socket CPU	Adapter
ET100-QF06 H8S/2214 H8S/2223 H8S/2225 H8S/2227 H8S/2233 H8S/2235 H8S/2236 H8S/2237 H8S/2238	**ET-1030 ET100-SET-QF06** **Surface Mountable Adapter for ET100 to QF06**  SIDE VIEW  TOP VIEW (all dimensions in mm)

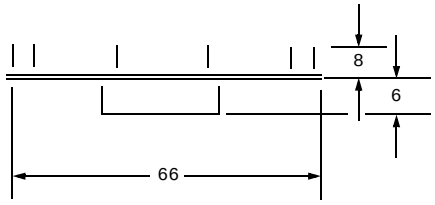
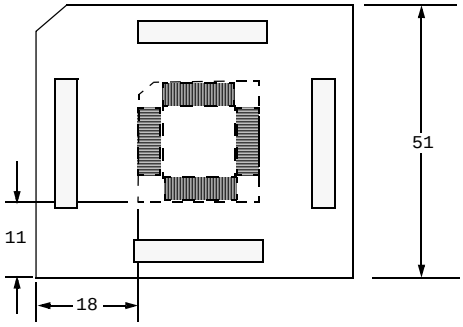
Socket CPU	Adapter
ET100-QF06 H8S/2214 H8S/2223 H8S/2225 H8S/2227 H8S/2233 H8S/2235 H8S/2236 H8S/2237 H8S/2238	**YA-1031 ET100-EYA-QF06** **Emul. Adapter for YAMAICHI socket ET100-QF06**  SIDE VIEW  TOP VIEW (all dimensions in mm)

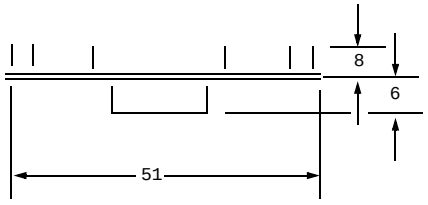
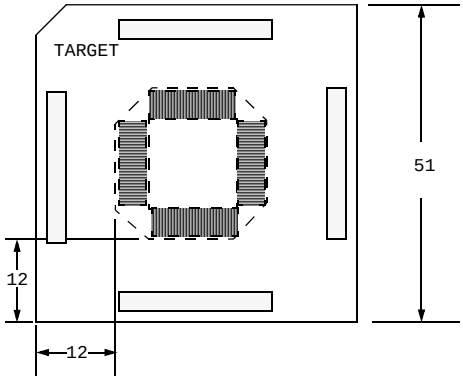
Socket CPU	Adapter
ET100-QF49 H8/3006 H8/3007 H8/3008 H8/3044 H8/3045 H8/3046 H8/3047 H8/3048 H8/3052 H8/3060 H8/3061 H8/3062 H8/3064 H8/3065 H8/3066 H8/3067 H8/3068 H8S/2142 H8S/2143 H8S/2144 H8S/2147 H8S/2148 H8S/2214 H8S/2223 H8S/2225 H8S/2227 H8S/2233 H8S/2235 H8S/2236 H8S/2237 H8S/2238 H8S/2240 H8S/2241 H8S/2242 H8S/2243 H8S/2244 H8S/2245 H8S/2246 H8S/2310 H8S/2311 H8S/2312 H8S/2316 H8S/2318 H8S/2319 H8S/2340 H8S/2341 H8S/2343 H8S/2345 H8S/2621 H8S/2622 H8S/2623 H8S/2626	**YA-1091 ET100-EYA-QF49** **Emul. Adapter for YAMAICHI socket ET100-QF49**  SIDE VIEW  TOP VIEW (all dimensions in mm)

Socket CPU	Adapter
ET120-QF56 H8S/2320 H8S/2322 H8S/2323 H8S/2324 H8S/2327 H8S/2328 H8S/2329 H8S/2350 H8S/2351 H8S/2352 H8S/2353 H8S/2355 H8S/2357 H8S/2631 H8S/2632 H8S/2633 H8S/2653 H8S/2655	**YA-1142 ET120-EYA-QF56** **Emul. Adapter for YAMAICHI socket ET120-QF56** 
ET128-QF51 H8S/2320 H8S/2322 H8S/2323 H8S/2324 H8S/2327 H8S/2328 H8S/2329 H8S/2350 H8S/2351 H8S/2352 H8S/2353 H8S/2355 H8S/2357 H8S/2631 H8S/2632 H8S/2633 H8S/2636 H8S/2639 H8S/2653 H8S/2655	**TO-1280 ET128-ETO-QF51** **Emul. Adapter for T0 socket ET128-QF51** 

Socket CPU	Adapter
ET144-QF63 H8S/2332 H8S/2337 H8S/2338 H8S/2339	**YA-1111 ET144-EYA-QF63** **Emul. Adapter for YAMAICHI socket ET144-QF63**  SIDE VIEW  TOP VIEW (all dimensions in mm)

Socket CPU	Adapter
ET64-QF29 H8/36014 H8/3664 H8/3672 H8/3687 H8/3694 H8S/2120 H8S/2122 H8S/2123 H8S/2124 H8S/2126 H8S/2127 H8S/2128	**YA-1121 ET64-EYA-QF29** **Emul. Adapter for YAMAICHI socket ET064-QF29**  SIDE VIEW  TOP VIEW (all dimensions in mm)

Socket CPU	Adapter
ET80-QF14 H8S/2130 H8S/2132 H8S/2133 H8S/2134 H8S/2137 H8S/2138 H8S/2612	**YA-1131 ET80-EYA-QF14** **Emul. Adapter for YAMAICHI socket ET080-QF14**  SIDE VIEW  TOP VIEW (all dimensions in mm)

Socket CPU	Adapter
ET80-QF47 H8S/2120 H8S/2122 H8S/2123 H8S/2124 H8S/2126 H8S/2127 H8S/2128 H8S/2130 H8S/2132 H8S/2133 H8S/2134 H8S/2137 H8S/2138	**YA-1081 ET80-EYA-QF47** **Emul. Adapter for YAMAICHI socket ET080-QF47**  SIDE VIEW  TOP VIEW (all dimensions in mm)

Operation Voltage

This list contains information on probes available for other voltage ranges. Probes not noted here supply an operation voltage range of 4.5 … 5.5 V.

CPU	Module	Adapter	Voltage Range
H8/3006	LA-9579	-	3.0 .. 5.5 V
H8/3007	LA-9579	-	3.0 .. 5.5 V
H8/3008	LA-9579	-	3.0 .. 5.5 V
H8/3044	LA-9579	-	3.0 .. 5.5 V
H8/3045	LA-9579	-	3.0 .. 5.5 V
H8/3046	LA-9579	-	3.0 .. 5.5 V
H8/3047	LA-9579	-	3.0 .. 5.5 V
H8/3048	LA-9579	-	3.0 .. 5.5 V
H8/3052	LA-9579	-	3.0 .. 5.5 V
H8/3060	LA-9579	-	3.0 .. 5.5 V
H8/3061	LA-9579	-	3.0 .. 5.5 V
H8/3062	LA-9579	-	3.0 .. 5.5 V
H8/3064	LA-9579	-	3.0 .. 5.5 V
H8/3065	LA-9579	-	3.0 .. 5.5 V
H8/3066	LA-9579	-	3.0 .. 5.5 V
H8/3067	LA-9579	-	3.0 .. 5.5 V
H8/3068	LA-9579	-	3.0 .. 5.5 V
H8/36014	LA-9569	-	3.0 .. 5.5 V
H8/3664	LA-9569	-	3.0 .. 5.5 V
H8/3672	LA-9569	-	3.0 .. 5.5 V
H8/3687	LA-9569	-	3.0 .. 5.5 V
H8/3694	LA-9569	-	3.0 .. 5.5 V
H8S/2120	LA-9573	-	3.0 .. 5.5 V
H8S/2122	LA-9573	-	3.0 .. 5.5 V
H8S/2123	LA-9573	-	3.0 .. 5.5 V
H8S/2124	LA-9573	-	3.0 .. 5.5 V
H8S/2126	LA-9573	-	3.0 .. 5.5 V
H8S/2127	LA-9573	-	3.0 .. 5.5 V
H8S/2128	LA-9573	-	3.0 .. 5.5 V
H8S/2130	LA-9572	-	3.0 .. 5.5 V
H8S/2132	LA-9572	-	3.0 .. 5.5 V
H8S/2133	LA-9572	-	3.0 .. 5.5 V
H8S/2134	LA-9572	-	3.0 .. 5.5 V
H8S/2137	LA-9572	-	3.0 .. 5.5 V
H8S/2138	LA-9572	-	3.0 .. 5.5 V
H8S/2142	LA-9572	-	3.0 .. 5.5 V

CPU	Module	Adapter	Voltage Range
H8S/2143	LA-9572	-	3.0 .. 5.5 V
H8S/2144	LA-9572	-	3.0 .. 5.5 V
H8S/2147	LA-9572	-	3.0 .. 5.5 V
H8S/2148	LA-9572	-	3.0 .. 5.5 V
H8S/2214	LA-9578	-	3.0 .. 3.6 V
H8S/2223	LA-9574	-	3.0 .. 3.6 V
H8S/2223	LA-9578	-	3.0 .. 3.6 V
H8S/2225	LA-9574	-	3.0 .. 3.6 V
H8S/2225	LA-9578	-	3.0 .. 3.6 V
H8S/2227	LA-9574	-	3.0 .. 3.6 V
H8S/2227	LA-9578	-	3.0 .. 3.6 V
H8S/2233	LA-9574	-	3.0 .. 3.6 V
H8S/2233	LA-9578	-	3.0 .. 3.6 V
H8S/2235	LA-9574	-	3.0 .. 3.6 V
H8S/2235	LA-9578	-	3.0 .. 3.6 V
H8S/2236	LA-9574	-	3.0 .. 3.6 V
H8S/2236	LA-9578	-	3.0 .. 3.6 V
H8S/2237	LA-9574	-	3.0 .. 3.6 V
H8S/2237	LA-9578	-	3.0 .. 3.6 V
H8S/2238	LA-9574	-	3.0 .. 3.6 V
H8S/2238	LA-9578	-	3.0 .. 3.6 V
H8S/2240	LA-9571	-	3.0 .. 5.5 V
H8S/2241	LA-9571	-	3.0 .. 5.5 V
H8S/2242	LA-9571	-	3.0 .. 5.5 V
H8S/2243	LA-9571	-	3.0 .. 5.5 V
H8S/2244	LA-9571	-	3.0 .. 5.5 V
H8S/2245	LA-9571	-	3.0 .. 5.5 V
H8S/2246	LA-9571	-	3.0 .. 5.5 V
H8S/2310	LA-9577	LA-9635	3.0 .. 3.5 V
H8S/2311	LA-9577	LA-9635	3.0 .. 3.5 V
H8S/2312	LA-9577	LA-9635	3.0 .. 3.5 V
H8S/2316	LA-9577	LA-9635	3.0 .. 3.5 V
H8S/2318	LA-9577	LA-9635	3.0 .. 3.5 V
H8S/2319	LA-9577	LA-9635	3.0 .. 3.5 V
H8S/2320	LA-9577	-	3.0 .. 3.6 V
H8S/2322	LA-9577	-	3.0 .. 3.6 V
H8S/2323	LA-9577	-	3.0 .. 3.6 V
H8S/2324	LA-9577	-	3.0 .. 3.6 V
H8S/2327	LA-9577	-	3.0 .. 3.6 V
H8S/2328	LA-9577	-	3.0 .. 3.6 V
H8S/2329	LA-9577	-	3.0 .. 3.6 V
H8S/2332	LA-9577	-	3.0 .. 3.6 V
H8S/2337	LA-9577	-	3.0 .. 3.6 V
H8S/2338	LA-9577	-	3.0 .. 3.6 V
H8S/2339	LA-9577	-	3.0 .. 3.6 V

CPU	Module	Adapter	Voltage Range
H8S/2340	LA-9571	LA-9635	3.0 .. 3.5 V
H8S/2341	LA-9571	LA-9635	3.0 .. 3.5 V
H8S/2343	LA-9571	LA-9635	3.0 .. 3.5 V
H8S/2345	LA-9571	LA-9635	3.0 .. 3.5 V
H8S/2350	LA-9571	-	3.0 .. 5.5 V
H8S/2351	LA-9571	-	3.0 .. 5.5 V
H8S/2352	LA-9571	-	3.0 .. 5.5 V
H8S/2353	LA-9571	-	3.0 .. 5.5 V
H8S/2355	LA-9571	-	3.0 .. 5.5 V
H8S/2357	LA-9571	-	3.0 .. 5.5 V
H8S/2621	LA-9576	-	3.0 .. 5.5 V
H8S/2622	LA-9576	-	3.0 .. 5.5 V
H8S/2623	LA-9576	-	3.0 .. 5.5 V
H8S/2626	LA-9576	-	3.0 .. 5.5 V
H8S/2631	LA-9576	-	3.0 .. 5.5 V
H8S/2632	LA-9576	-	3.0 .. 5.5 V
H8S/2633	LA-9576	-	3.0 .. 5.5 V
H8S/2653	LA-9571	-	3.0 .. 5.5 V
H8S/2655	LA-9571	-	3.0 .. 5.5 V

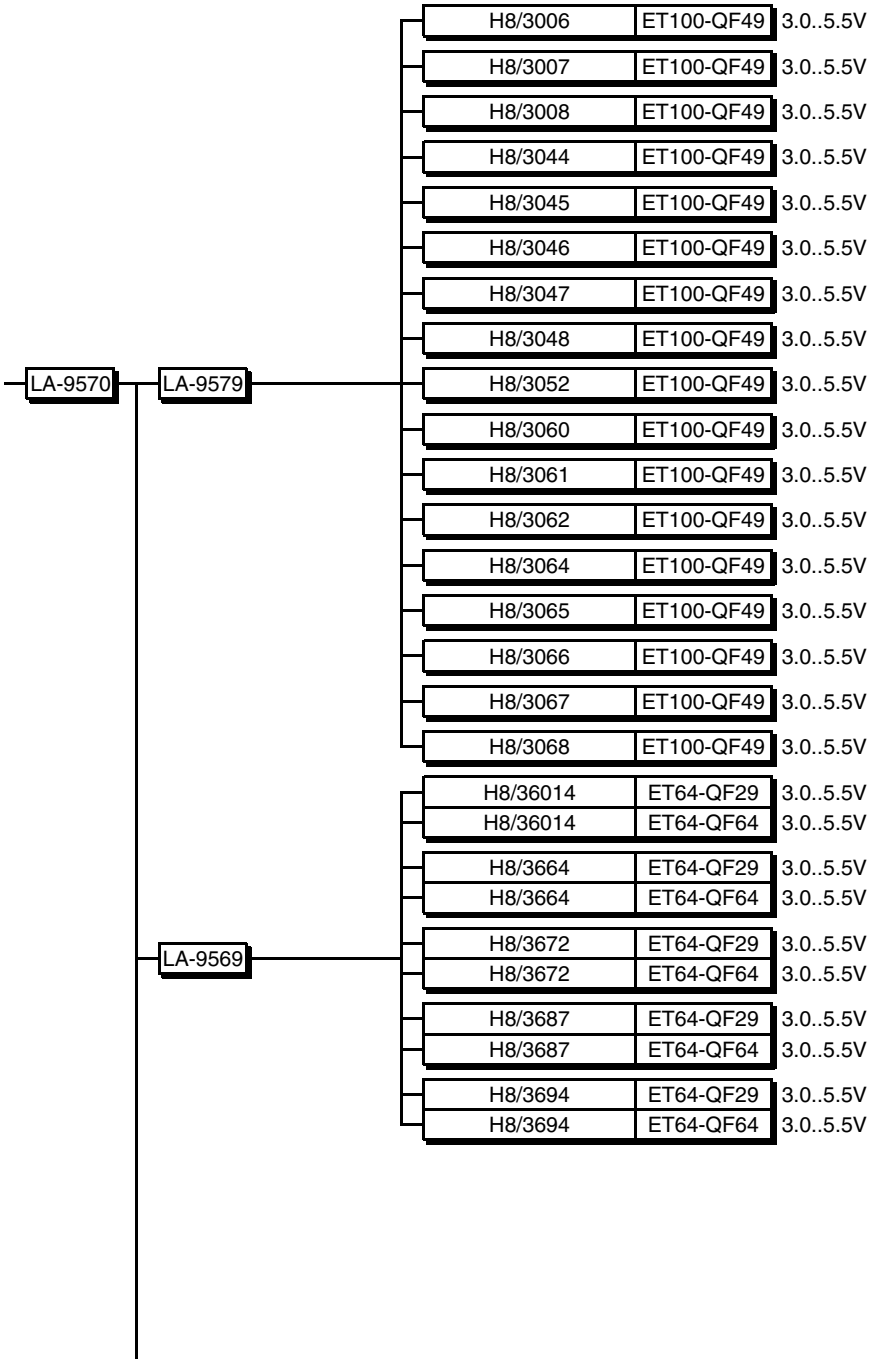
Operation Frequency

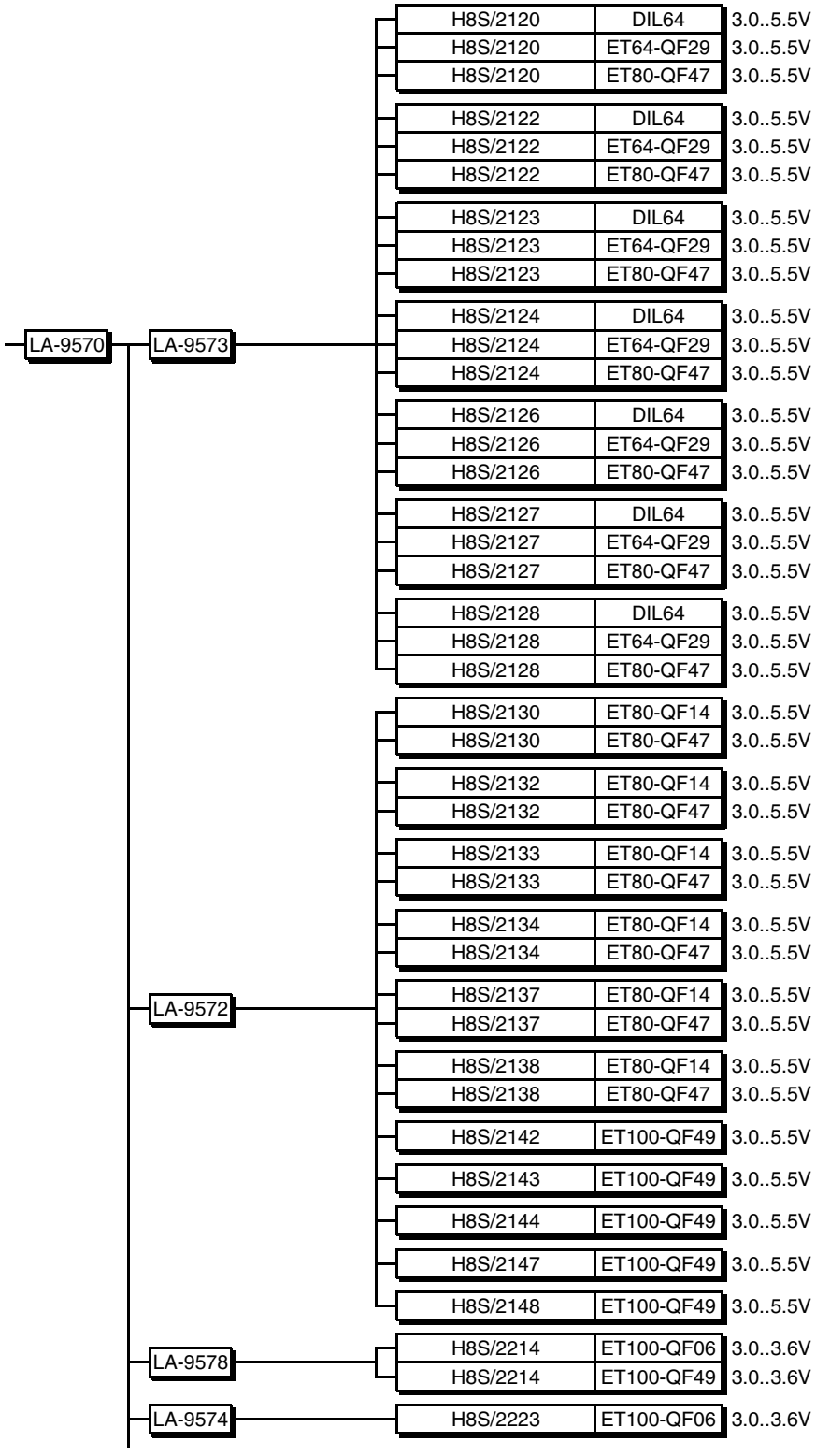
Module	CPU	F-W0-10	F-W1-10	S-W0-10	S-W1-10	CHIP	TRACE	HEAD RAM
LA-9579	H8/3006	35.0	35.0+	28.0	35.0+	35.0	*	*
LA-9579	H8/3007	35.0	35.0+	28.0	35.0+	35.0	*	*
LA-9579	H8/3008	35.0	35.0+	28.0	35.0+	35.0	*	*
LA-9579	H8/3044	35.0	35.0+	28.0	35.0+	35.0	*	*
LA-9579	H8/3045	35.0	35.0+	28.0	35.0+	35.0	*	*
LA-9579	H8/3046	35.0	35.0+	28.0	35.0+	35.0	*	*
LA-9579	H8/3047	35.0	35.0+	28.0	35.0+	35.0	*	*
LA-9579	H8/3048	35.0	35.0+	28.0	35.0+	35.0	*	*
LA-9579	H8/3052	35.0	35.0+	28.0	35.0+	35.0	*	*
LA-9579	H8/3060	35.0	35.0+	28.0	35.0+	35.0		
LA-9579	H8/3061	35.0	35.0+	28.0	35.0+	35.0		
LA-9579	H8/3062	35.0	35.0+	28.0	35.0+	35.0		
LA-9579	H8/3064	35.0	35.0+	28.0	35.0+	35.0		
LA-9579	H8/3065	35.0	35.0+	28.0	35.0+	35.0		
LA-9579	H8/3066	35.0	35.0+	28.0	35.0+	35.0		
LA-9579	H8/3067	35.0	35.0+	28.0	35.0+	35.0		
LA-9579	H8/3068	35.0	35.0+	28.0	35.0+	35.0		
LA-9569	H8/36014	35.0	35.0+	28.0	35.0+	35.0		
LA-9569	H8/3664	35.0	35.0+	28.0	35.0+	35.0		

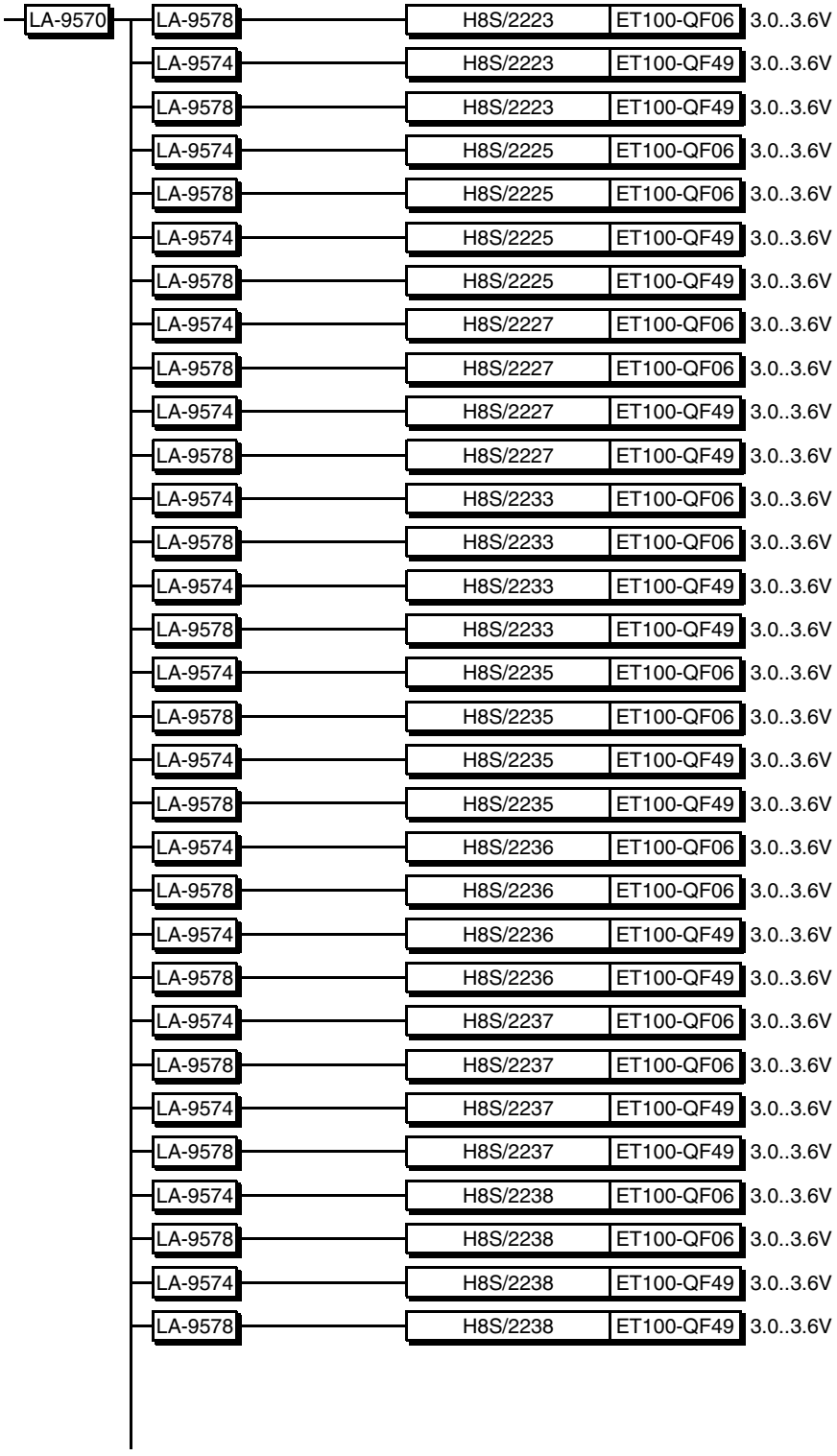
Module	CPU	F-W0-10	F-W1-10	S-W0-10	S-W1-10	CHIP	TRACE	HEAD RAM
LA-9569	H8/3672	35.0	35.0+	28.0	35.0+	35.0		
LA-9569	H8/3687	35.0	35.0+	28.0	35.0+	35.0		
LA-9569	H8/3694	35.0	35.0+	28.0	35.0+	35.0		
LA-9573	H8S/2120	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9573	H8S/2122	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9573	H8S/2123	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9573	H8S/2124	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9573	H8S/2126	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9573	H8S/2127	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9573	H8S/2128	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9572	H8S/2130	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9572	H8S/2132	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9572	H8S/2133	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9572	H8S/2134	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9572	H8S/2137	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9572	H8S/2138	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9572	H8S/2142	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9572	H8S/2143	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9572	H8S/2144	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9572	H8S/2147	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9572	H8S/2148	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9578	H8S/2214	13.0	13.0+	11.9	13.0+	13.0		
LA-9574	H8S/2223	13.0	13.0+	11.9	13.0+	13.0	*	*
LA-9574	H8S/2225	13.0	13.0+	11.9	13.0+	13.0	*	*
LA-9574	H8S/2227	13.0	13.0+	11.9	13.0+	13.0	*	*
LA-9574	H8S/2233	13.0	13.0+	11.9	13.0+	13.0	*	*
LA-9574	H8S/2235	13.0	13.0+	11.9	13.0+	13.0	*	*
LA-9574	H8S/2236	13.0	13.0+	11.9	13.0+	13.0	*	*
LA-9574	H8S/2237	13.0	13.0+	11.9	13.0+	13.0	*	*
LA-9574	H8S/2238	13.0	13.0+	11.9	13.0+	13.0	*	*
LA-9571	H8S/2240	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9571	H8S/2241	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9571	H8S/2242	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9571	H8S/2243	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9571	H8S/2244	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9571	H8S/2245	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9571	H8S/2246	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9577	H8S/2310	25.0	25.0+	21.2	25.0+	25.0		
LA-9577	H8S/2311	25.0	25.0+	21.2	25.0+	25.0		
LA-9577	H8S/2312	25.0	25.0+	21.2	25.0+	25.0		
LA-9577	H8S/2316	25.0	25.0+	21.2	25.0+	25.0		
LA-9577	H8S/2318	25.0	25.0+	21.2	25.0+	25.0		
LA-9577	H8S/2319	25.0	25.0+	21.2	25.0+	25.0	*	*
LA-9577	H8S/2320	25.0	25.0+	21.2	25.0+	25.0		

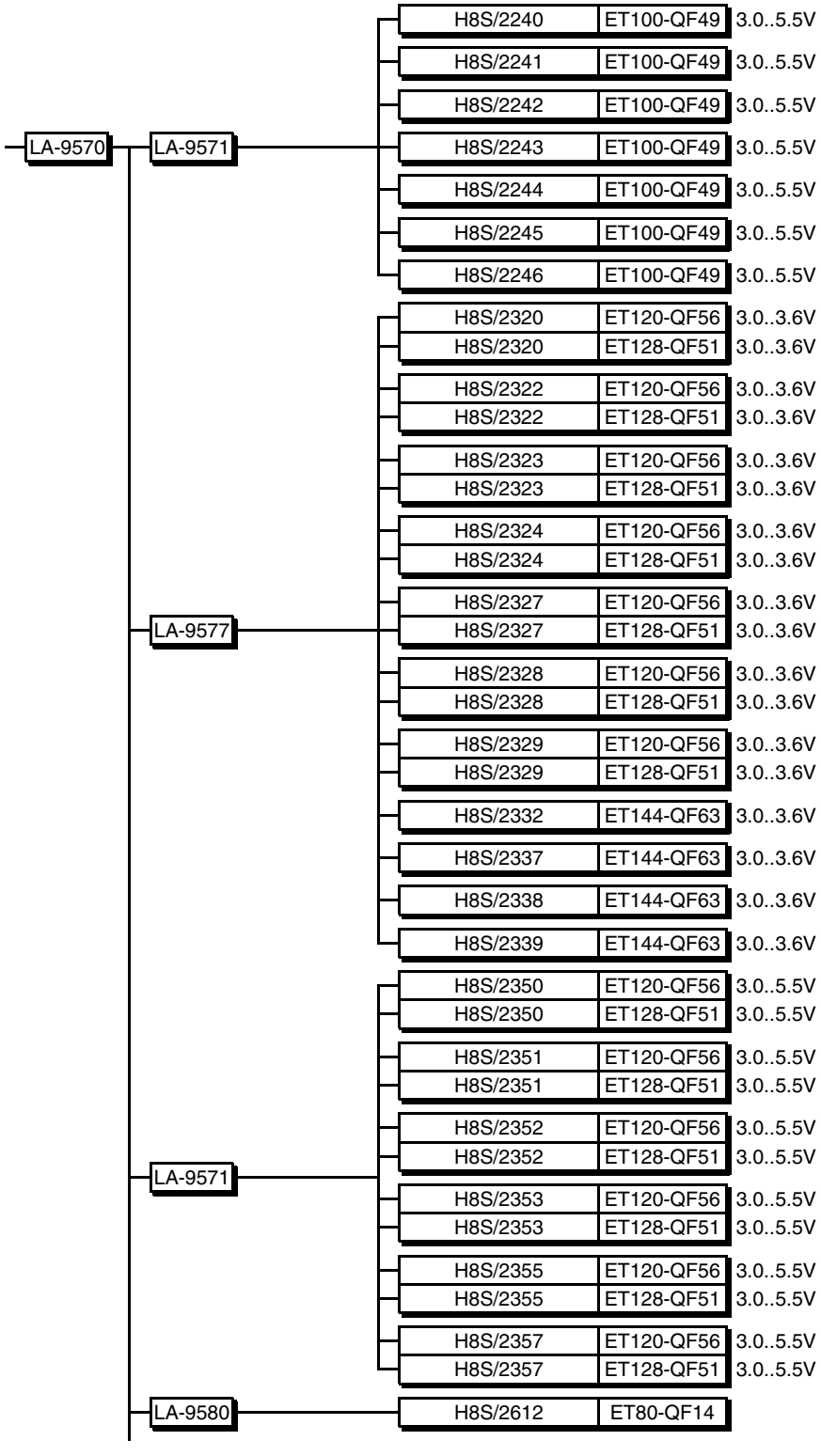
Module	CPU	F-W0-10	F-W1-10	S-W0-10	S-W1-10	CHIP	TRACE	HEAD RAM
LA-9577	H8S/2322	25.0	25.0+	21.2	25.0+	25.0	*	*
LA-9577	H8S/2323	25.0	25.0+	21.2	25.0+	25.0	*	*
LA-9577	H8S/2324	25.0	25.0+	21.2	25.0+	25.0		
LA-9577	H8S/2327	25.0	25.0+	21.2	25.0+	25.0	*	*
LA-9577	H8S/2328	25.0	25.0+	21.2	25.0+	25.0	*	*
LA-9577	H8S/2329	25.0	25.0+	21.2	25.0+	25.0	*	*
LA-9577	H8S/2332	25.0	25.0+	21.2	25.0+	25.0	*	*
LA-9577	H8S/2337	25.0	25.0+	21.2	25.0+	25.0	*	*
LA-9577	H8S/2338	25.0	25.0+	21.2	25.0+	25.0	*	*
LA-9577	H8S/2339	25.0	25.0+	21.2	25.0+	25.0	*	*
LA-9571	H8S/2340	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9571	H8S/2341	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9571	H8S/2343	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9571	H8S/2345	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9571	H8S/2350	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9571	H8S/2351	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9571	H8S/2352	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9571	H8S/2353	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9571	H8S/2355	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9571	H8S/2357	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9580	H8S/2612	20.0	20.0+	17.5	20.0+	20.0		
LA-9576	H8S/2621	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9576	H8S/2622	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9576	H8S/2623	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9576	H8S/2626	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9576	H8S/2631	25.0	25.0+	21.2	25.0+	25.0	*	*
LA-9576	H8S/2632	25.0	25.0+	21.2	25.0+	25.0	*	*
LA-9576	H8S/2633	25.0	25.0+	21.2	25.0+	25.0	*	*
LA-9575	H8S/2636	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9575	H8S/2639	20.0	20.0+	17.5	20.0+	20.0		
LA-9571	H8S/2653	20.0	20.0+	17.5	20.0+	20.0	*	*
LA-9571	H8S/2655	20.0	20.0+	17.5	20.0+	20.0	*	*

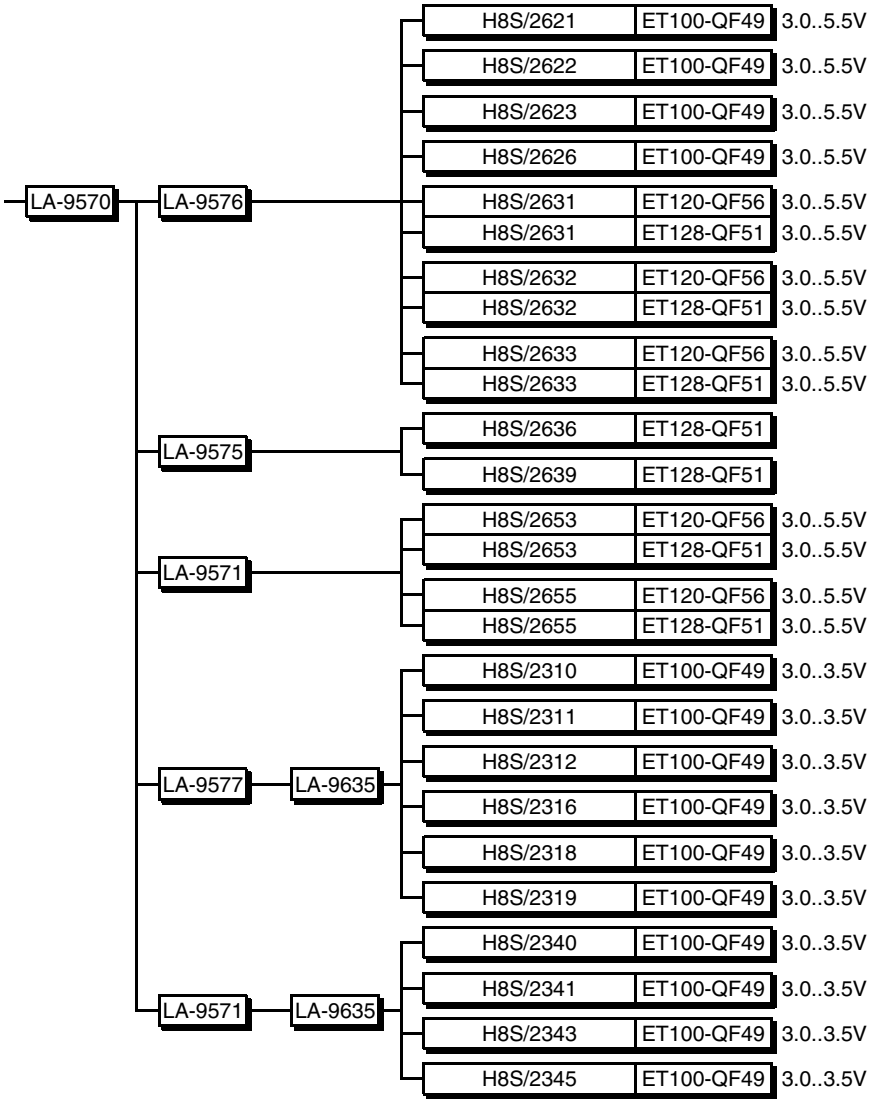
Probes











CPU	ICE	FIRE	ICD DEBUG	ICD MONITOR	ICD TRACE	POWER INTEGRATOR	INSTRUCTION SIMULATOR
H8/3006	YES	YES		YES			YES
H8/3007	YES	YES		YES			YES
H8/3008		YES		YES			YES
H8/3044		YES		YES			YES
H8/3045		YES		YES			YES
H8/3046		YES		YES			YES
H8/3047		YES		YES			YES
H8/3048		YES		YES			YES
H8/3052		YES		YES			YES
H8/3060	YES	YES		YES			YES
H8/3061	YES	YES		YES			YES
H8/3062	YES	YES		YES			YES
H8/3064	YES	YES		YES			YES
H8/3065	YES	YES		YES			YES
H8/3066	YES	YES		YES			YES
H8/3067	YES	YES		YES			YES
H8/3068		YES		YES			YES
H8/36014		YES					YES
H8/3664		YES					YES
H8/3672		YES					YES
H8/3687		YES					YES
H8/3694		YES					YES
H8S/2120		YES		YES			YES
H8S/2122		YES		YES			YES
H8S/2123		YES		YES			YES
H8S/2124		YES		YES			YES
H8S/2126		YES		YES			YES
H8S/2127		YES		YES			YES
H8S/2128		YES		YES			YES
H8S/2130		YES		YES			YES
H8S/2132		YES		YES			YES
H8S/2133		YES		YES			YES
H8S/2134		YES		YES			YES
H8S/2137		YES		YES			YES
H8S/2138		YES		YES			YES
H8S/2142		YES		YES			YES
H8S/2143		YES		YES			YES
H8S/2144		YES		YES			YES

CPU	ICE	FIRE	ICD DEBUG	ICD MONITOR	ICD TRACE	POWER INTEGRATOR	INSTRUCTION SIMULATOR
H8S/2147		YES		YES			YES
H8S/2148		YES		YES			YES
H8S/2214		YES		YES			YES
H8S/2223		YES		YES			YES
H8S/2225		YES		YES			YES
H8S/2227		YES		YES			YES
H8S/2233		YES		YES			YES
H8S/2235		YES		YES			YES
H8S/2236		YES		YES			YES
H8S/2237		YES		YES			YES
H8S/2238		YES		YES			YES
H8S/2240		YES		YES			YES
H8S/2241		YES		YES			YES
H8S/2242		YES		YES			YES
H8S/2243		YES		YES			YES
H8S/2244		YES		YES			YES
H8S/2245		YES		YES			YES
H8S/2246		YES		YES			YES
H8S/2310		YES		YES			YES
H8S/2311		YES		YES			YES
H8S/2312		YES		YES			YES
H8S/2316		YES		YES			YES
H8S/2318		YES		YES			YES
H8S/2319		YES		YES			YES
H8S/2320		YES		YES			YES
H8S/2322		YES		YES			YES
H8S/2323		YES		YES			YES
H8S/2324		YES		YES			YES
H8S/2327		YES		YES			YES
H8S/2328		YES		YES			YES
H8S/2329		YES		YES			YES
H8S/2332		YES		YES			YES
H8S/2337		YES		YES			YES
H8S/2338		YES		YES			YES
H8S/2339		YES		YES			YES
H8S/2340		YES		YES			YES
H8S/2341		YES		YES			YES
H8S/2343		YES		YES			YES
H8S/2345		YES		YES			YES
H8S/2350		YES		YES			YES
H8S/2351		YES		YES			YES

CPU	ICE	FIRE	ICD DEBUG	ICD MONITOR	ICD TRACE	POWER INTEGRATOR	INSTRUCTION SIMULATOR
H8S/2352		YES		YES			YES
H8S/2353		YES		YES			YES
H8S/2355		YES		YES			YES
H8S/2357		YES		YES			YES
H8S/2612		YES		YES			YES
H8S/2621		YES		YES			YES
H8S/2622		YES		YES			YES
H8S/2623		YES		YES			YES
H8S/2626		YES		YES			YES
H8S/2631		YES		YES			YES
H8S/2632		YES		YES			YES
H8S/2633		YES		YES			YES
H8S/2636		YES		YES			YES
H8S/2639		YES		YES			YES
H8S/2653		YES		YES			YES
H8S/2655		YES		YES			YES

Compilers

Language	Compiler	Company	Option	Comment
C	ICCH8	IAR Systems AB	UBROF	H8S
C	CH38	Renesas Technology, Corp.	SYSROF	H8S
C++	GNU	Free Software Foundation, Inc.	COFF	
C++	CH38	Renesas Technology, Corp.	SYSROF	

Realtime Operation Systems

Name	Company	Comment
CMX-RTX	CMX Systems Inc.	
CMX-TINY	CMX Systems Inc.	
FreeRTOS	Freeware I	v7
Nucleus PLUS	Mentor Graphics Corporation	
osCAN	Vector	via ORTI
OSEK	-	via ORTI
ProOSEK	Elektrobit Automotive GmbH	via ORTI
RTXC 3.2	Quadros Systems Inc.	

3rd Party Tool Integrations

CPU	Tool	Company	Host
ALL	ADENEO	Adeneo Embedded	
ALL	X-TOOLS / X32	blue river software GmbH	Windows
ALL	CODEWRIGHT	Borland Software Corporation	Windows
ALL	CODE CONFIDENCE TOOLS	Code Confidence Ltd	Windows
ALL	CODE CONFIDENCE TOOLS	Code Confidence Ltd	Linux
ALL	EASYCODE	EASYCODE GmbH	Windows
ALL	ECLIPSE	Eclipse Foundation, Inc	Windows
ALL	RHAPSODY IN MICROC	IBM Corp.	Windows
ALL	RHAPSODY IN C++	IBM Corp.	Windows
ALL	LDRA TOOL SUITE	LDRA Technology, Inc.	Windows
ALL	ATTOL TOOLS	MicroMax Inc.	Windows
ALL	VISUAL BASIC INTERFACE	Microsoft Corporation	Windows
ALL	LABVIEW	NATIONAL INSTRUMENTS Corporation	Windows
ALL	CODE::BLOCKS	Open Source	-
ALL	C++TEST	Parasoft	Windows

CPU	Tool	Company	Host
ALL	RAPITIME	Rapita Systems Ltd.	Windows
ALL	DA-C	RistanCASE	Windows
ALL	SIMULINK	The MathWorks Inc.	Windows
ALL	VECTORCAST/RSP	Vector Software	Windows
ALL	WINDOWS CE PLATF. BUILDER	Windows	Windows

Product Information

OrderNo Code	Text
LA-9570 FIRE-H8S	**FIRE Family Module for H8S, H8Tiny, H8/300H** includes 512KByte Break and Emulation RAM requires FIRE-SRAM
LA-9571 FIRE-M-H8S-1	**FIRE CPU Module for H8S/265x/235x/234x/224x** QFP128, TQFP120 Adapter for H8S/2655/2653 H8S/2357F/2357/2355/2353/2352/2351/2350 H8S/2390/2392/2394/2398 QFP128 requires ET128-QF51 TQFP120 requires ET120-QF56 QFP100, TQFP100 Adapter for H8S/2246/2245/2244/2243/2242/2241/2240 QFP100, TQFP100 requires ET100-QF49 Via Adapter LA-9635 (ET128QF51-ET100QF49) H8S/2345/2343/2341/2340 QFP100, TQFP100 requires ET100-QF49
LA-9572 FIRE-M-H8S-2	**FIRE CPU Module for H8S/214x/213x** QFP100, TQFP100 Adapter for H8S/2148/2147/2144/2143/2142 QFP100, TQFP100 requires ET100-QF49 QFP80, TQFP80 Adapter for H8S/2138/2137/2134/2133/2132/2130 QFP80 requires ET80-QF14 TQFP80 requires ET80-QF47
LA-9573 FIRE-M-H8S-3	**FIRE CPU Module for H8S/212x** DIL64, QFP64, TQFP80 Adapter for H8S/2128/2127/2126/2124/2123/2122/2120 QFP64 requires ET64-QF29 TQFP80 requires ET80-QF47
LA-9574 FIRE-M-H8S-4	**FIRE CPU Module for H8S/222x/223x** QFP100, TQFP100 Adapter for H8S/2223/2225/2227/2233/2235/2236/2237/2238 QFP100 (0.65mm) requires ET100-QF06 QFP100, TQFP100 (0.5mm) requires ET100-QF49 TQFP100 (0.4mm) requires ET100-SE
LA-9575 FIRE-M-H8S-5	**FIRE CPU Module for H8S/2636/2639** QFP128 Adapter for H8S/2636, H8S/2639 QFP128 requires ET128-QF51
LA-9576 FIRE-M-H8S-6	**FIRE CPU Module for H8S/262x/263x** QFP128, TQFP120 Adapter for H8S/2631/2632/2633 QFP128 requires ET128-QF51 TQFP120 requires ET120-QF56 QFP100 Adapter for H8S/2621/2622/2623/2626 QFP100 requires ET100-QF49
LA-9577 FIRE-M-H8S-7	**FIRE CPU Module for H8S/231x/232x/233x** QFP128, TQFP120 Adapter for H8S/2320/2322/2323/2324/2327/2328/2329 QFP128 requires ET128-QF51 TQFP120 requires ET120-QF56 QFP144 Adapter for H8S/2332/2337/2338/2339 QFP144 requires ET144-QF63 Via Adapter LA-9635 (ET128QF51-ET100QF49) H8S/2310/2311/2312/2316/2318 QFP100, TQFP100 requires ET100-QF49

OrderNo Code	Text
LA-9578 FIRE-M-H8S-8	**FIRE CPU Module for H8S/2214/222x/223x** QFP100, TQFP100 Adapter for H8S/2214/2223/2225/2227/2233/2235/2236/2237/2238 QFP100 (0.65mm) requires ET100-QF06 QFP100, TQFP100 (0.5mm) requires ET100-QF49 TQFP100 (0.4mm) requires ET100-SE
LA-9635 A-H8S/234X/231X	**Converter ET128QF51 to ET100QF49 for H8S/234x** Adapter for 235x (ET128QF51) to 234x (ET100QF49) Converter Et128QF51 to ET100QF49
LA-9579 FIRE-M-H8S-9	**FIRE CPU Module for H8/3069** H8/3006/3007/3008 H8/3044/3045/3046/3047/3048 H8/3052 H8/3060/3061/3062/3064/3065/3066/3067/3068 requires ET100-QF49 (0.5 pitch)
LA-9580 FIRE-M-H8S-10	**FIRE CPU Module for H8S/2612** requires ET80-QF14 Adapter for H8S/2612
LA-9569 FIRE-M-H8S-11	**FIRE CPU Module for H8/3664** H8/3664 requires ET64-QF64 or ET64-QF29 H8/3672 requires ET64-QF64 H8/3687 requires ET64-QF64 or ET64-QF29 H8/3694 requires ET64-QF64 or ET64-QF29 H8/36014 requires ET64-QF64
LA-9586 FIRE-M-H8S-12	**FIRE CPU Module for H8S/214xB/213xB** QFP100, TQFP100 Adapter for H8S/2148/2147/2144/2143/2142 H8S/2148B/2147B/2144B/2143B/2142B QFP100, TQFP100 requires ET100-QF49 QFP80, TQFP80 Adapter for H8S/2138/2137/2134/2133/2132/2130 H8S/2138B/2137B/2134B/2133B/2132B/2130B QFP80 requires ET80-QF14 TQFP80 requires ET80-QF47
LA-9587 FIRE-M-H8S-13	**FIRE CPU Module for H8S/237x/266x/267x** QFP144 Adapter for H8S/2670/2673/2674R/2675/2676 H8S/2375/2376/2377/2378 H8S/2375R/2377R/2378R H8S/2668 QFP144 requires ET144-QF63
LA-9588 FIRE-M-H8S-14	**FIRE CPU Module for H8S/236x** QFP128/QFP120 Adapter for H8S/2365/2366/2367/2368 H8S/2365R/2367R/2368R QFP120 requires ET120-QF56 QFP128 requires ET128-QF51

Order Information

Order No.	Code	Text
LA-9570	**FIRE-H8S**	**FIRE Family Module for H8S, H8Tiny, H8/300H**
LA-9571	**FIRE-M-H8S-1**	**FIRE CPU Module for H8S/265x/235x/234x/224x**
LA-9572	**FIRE-M-H8S-2**	**FIRE CPU Module for H8S/214x/213x**
LA-9573	**FIRE-M-H8S-3**	**FIRE CPU Module for H8S/212x**
LA-9574	**FIRE-M-H8S-4**	**FIRE CPU Module for H8S/222x/223x**
LA-9575	**FIRE-M-H8S-5**	**FIRE CPU Module for H8S/2636/2639**
LA-9576	**FIRE-M-H8S-6**	**FIRE CPU Module for H8S/262x/263x**
LA-9577	**FIRE-M-H8S-7**	**FIRE CPU Module for H8S/231x/232x/233x**
LA-9578	**FIRE-M-H8S-8**	**FIRE CPU Module for H8S/2214/222x/223x**
LA-9635	**A-H8S/234X/231X**	**Converter ET128QF51 to ET100QF49 for H8S/234x**
LA-9579	**FIRE-M-H8S-9**	**FIRE CPU Module for H8/3069**
LA-9580	**FIRE-M-H8S-10**	**FIRE CPU Module for H8S/2612**
LA-9569	**FIRE-M-H8S-11**	**FIRE CPU Module for H8/3664**
LA-9586	**FIRE-M-H8S-12**	**FIRE CPU Module for H8S/214xB/213xB**
LA-9587	**FIRE-M-H8S-13**	**FIRE CPU Module for H8S/237x/266x/267x**
LA-9588	**FIRE-M-H8S-14**	**FIRE CPU Module for H8S/236x**
Additional Options		
TO-1260	ET100-ETO-QF06	Emul. Adapter for TO socket ET100-QF06
TO-1250	ET100-ETO-QF49	Emul. Adapter for T0 socket ET100-QF49
TO-1255	ET100-ETO-SE	Emul. Adapter for T0 socket ET100-SE 0.4mm
YA-1031	ET100-EYA-QF06	Emul. Adapter for YAMAICHI socket ET100-QF06
YA-1091	ET100-EYA-QF49	Emul. Adapter for YAMAICHI socket ET100-QF49
ET-1030	ET100-SET-QF06	Surface Mountable Adapter for ET100 to QF06
ET-1092	ET100-SET-QF49	Surface Mountable Adapter for ET100-QF49
TO-1261	ET100-STO-QF06	Emul. Adapter TO-surface mount. ET100-QF06
TO-1251	ET100-STO-QF49	Emul. Adapter TO-surface mount. ET100-QF49
YA-1142	ET120-EYA-QF56	Emul. Adapter for YAMAICHI socket ET120-QF56
TO-1280	ET128-ETO-QF51	Emul. Adapter for T0 socket ET128-QF51
TO-1281	ET128-STO-QF51	Emul. Adapter TO-surface mount. ET128-QF51
TO-1310	ET144-ETO-QF63	Emul. Adapter for T0 socket ET144-QF63
YA-1111	ET144-EYA-QF63	Emul. Adapter for YAMAICHI socket ET144-QF63
ET-1110	ET144-SET-QF63	Surface Mountable Adapter for ET144-QF63
TO-1311	ET144-STO-QF63	Emul. Adapter TO-surface mount. ET144-QF63
TO-1240	ET64-ETO-QF29	Emul. Adapter for T0 socket ET64-QF29
TO-1245	ET64-ETO-QF64	Emul. Adapter for T0 socket ET64-QF64
YA-1121	ET64-EYA-QF29	Emul. Adapter for YAMAICHI socket ET064-QF29
ET-1122	ET64-SET-QF29	Surface Mountable Adapter for QF29
TO-1241	ET64-STO-QF29	Emul. Adapter TO-surface mount. ET64-QF29
TO-1275	ET80-ETO-QF14	Emul. Adapter for T0 socket ET080-QF14

Order No.	Code	Text
TO-1270	ET80-ETO-QF47	Emul. Adapter for T0 socket ET080-QF47
YA-1131	ET80-EYA-QF14	Emul. Adapter for YAMAICHI socket ET080-QF14
YA-1081	ET80-EYA-QF47	Emul. Adapter for YAMAICHI socket ET080-QF47
ET-1130	ET80-SET-QF14	Surface Mountable Adapter for ET80-QF14
TO-1276	ET80-STO-QF14	Emul. Adapter TO-surface mount. ET080-QF14
TO-1271	ET80-STO-QF47	Emul. Adapter TO-surface mount. ET080-QF47
LA-7528	MON-H8	ROM Monitor for H8/300H and H8S family on ESI
LA-8808	SIM-H8	TRACE32 Instruction Set Simulator for H8/H8S
YA-1162	YA-SOCKET-QF56	YAMAICHI Socket ET120-QF56